

1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™¹ technology, featuring very low on-state resistance.

Product availability:

BUK9275-100A in SOT428 (D-PAK).

2. Features

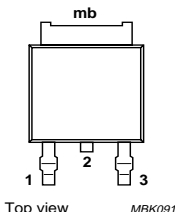
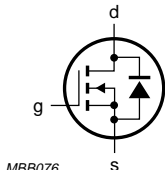
- TrenchMOS™ technology
- Q101 compliant
- 175 °C rated
- Logic level compatible.

3. Applications

- Automotive and general purpose power switching:
 - ◆ 12 V, 24 V and 42 V loads
 - ◆ Motors, lamps and solenoids.

4. Pinning information

Table 1: Pinning - SOT428 (D-PAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 <p>Top view MBK091</p>	 <p>MBB076</p>
2	drain (d)		
3	source (s)		
mb	mounting base; connected to drain (d)		
		SOT428 (D-PAK)	

1. TrenchMOS is a trademark of Royal Philips Electronics.

5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V _{DS}	drain-source voltage (DC)		–	100	V
I _D	drain current (DC)	T _{mb} = 25 °C; V _{GS} = 5 V	–	21.7	A
P _{tot}	total power dissipation	T _{mb} = 25 °C	–	88	W
T _j	junction temperature		–	175	°C
R _{DSon}	drain-source on-state resistance	T _j = 25 °C; V _{GS} = 5 V; I _D = 10 A	64	75	mΩ
		T _j = 25 °C; V _{GS} = 4.5 V; I _D = 10 A	–	84	mΩ

6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage (DC)		–	100	V
V _{DGR}	drain-gate voltage (DC)	R _{GS} = 20 kΩ	–	100	V
V _{GS}	gate-source voltage (DC)		–	±10	V
V _{GSM}	non-repetitive gate-source voltage	t _p ≤ 50 μs	–	±15	V
I _D	drain current (DC)	T _{mb} = 25 °C; V _{GS} = 5 V; Figure 2 and 3	–	21.7	A
		T _{mb} = 100 °C; V _{GS} = 5 V; Figure 2	–	15.3	A
I _{DM}	peak drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs; Figure 3	[1] –	87	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Figure 1	–	88	W
T _{stg}	storage temperature		–55	+175	°C
T _j	operating junction temperature		–55	+175	°C

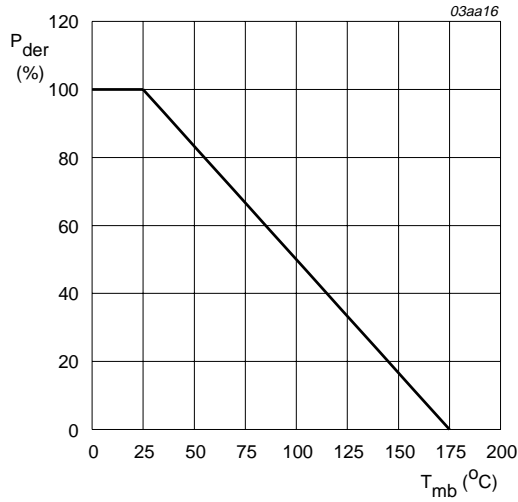
Source-drain diode

I _{DR}	reverse drain current (DC)	T _{mb} = 25 °C	–	21.7	A
I _{DRM}	pulsed reverse drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs	–	87	A

Avalanche ruggedness

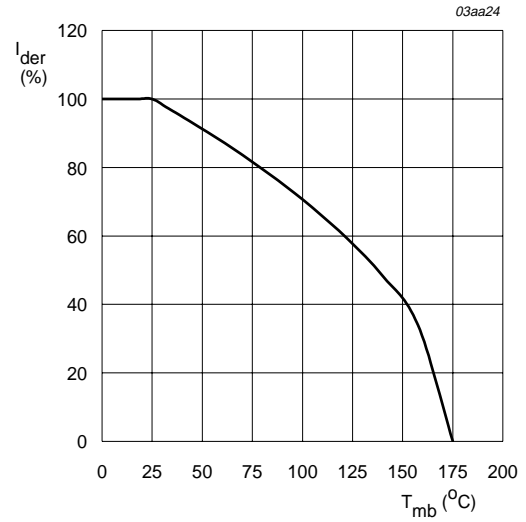
W _{DSS}	non-repetitive avalanche energy	unclamped inductive load; I _D = 14 A; V _{DS} ≤ 100 V; V _{GS} = 5 V; R _{GS} = 50 Ω; starting T _j = 25 °C	–	100	mJ
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[1] I_{DM} is limited by chip, not package.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

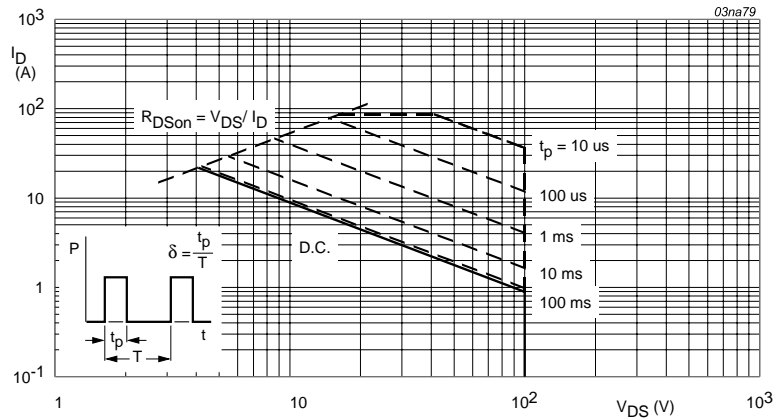
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$V_{GS} \geq 4.5 \text{ V}$$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{amb} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Figure 4	71.4	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		1.7	K/W

7.1 Transient thermal impedance

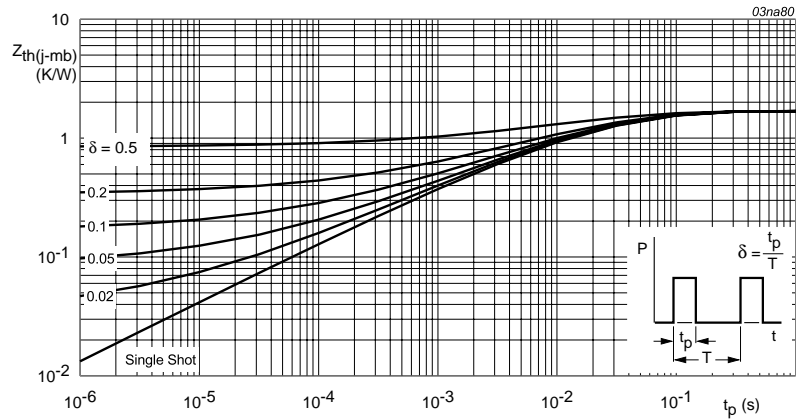


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

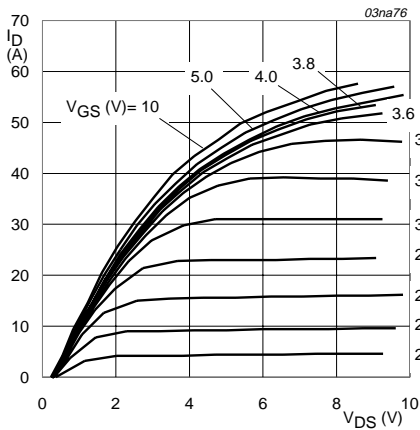
Table 5: Characteristics
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V T _j = 25 °C	100	–	–	V
		T _j = –55 °C	89	–	–	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9				
		T _j = 25 °C	1	1.5	2	V
		T _j = 175 °C	0.5	–	–	V
		T _j = –55 °C	–	–	2.3	V
I _{DSS}	drain-source leakage current	V _{DS} = 100 V; V _{GS} = 0 V T _j = 25 °C	–	0.05	10	μA
		T _j = 175 °C	–	–	500	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±10 V; V _{DS} = 0 V	–	2	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 10 A; Figure 7 and 8				
		T _j = 25 °C	–	64	75	mΩ
		T _j = 175 °C	–	–	188	mΩ
		V _{GS} = 4.5 V; I _D = 10 A	–	–	84	mΩ
		V _{GS} = 10 V; I _D = 10 A	–	62	72	mΩ
Dynamic characteristics						
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V;	–	1268	1690	pF
C _{oss}	output capacitance	f = 1 MHz; Figure 12	–	139	167	pF
C _{rss}	reverse transfer capacitance		–	90	124	pF
t _{d(on)}	turn-on delay time	V _{DD} = 30 V; R _L = 1.2 Ω;	–	13	–	ns
t _r	rise time	V _{GS} = 5 V; R _G = 10 Ω;	–	120	–	ns
t _{d(off)}	turn-off delay time		–	58	–	ns
t _f	fall time		–	57	–	ns
L _d	internal drain inductance	measured from drain lead from package to centre of die	–	2.5	–	nH
L _s	internal source inductance	measured from source lead from package to source bond pad	–	7.5	–	nH

Table 5: Characteristics...continued

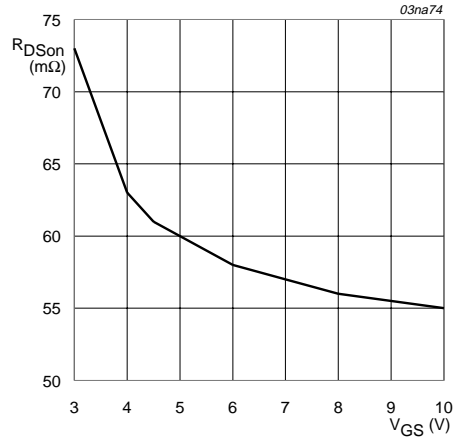
$T_j = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 10\text{ A}; V_{GS} = 0\text{ V};$ Figure 15	–	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}$	–	63	–	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}; V_{DS} = 30\text{ V}$	–	220	–	nC



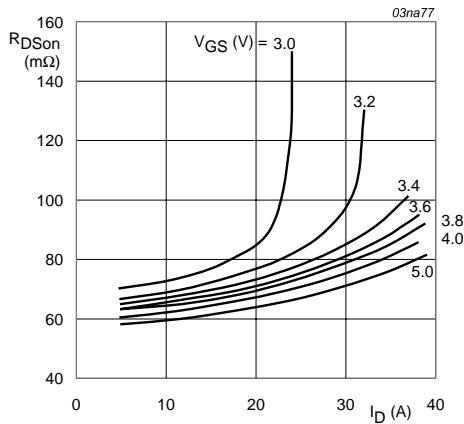
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



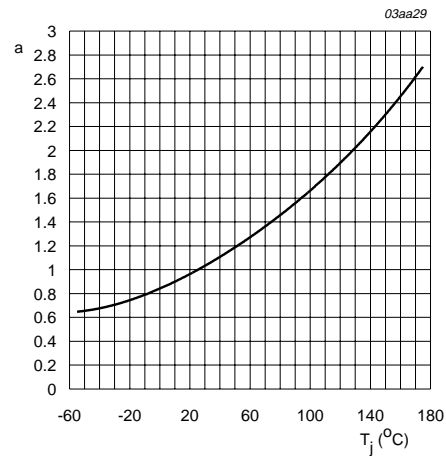
$T_j = 25^\circ\text{C}; I_D = 13\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



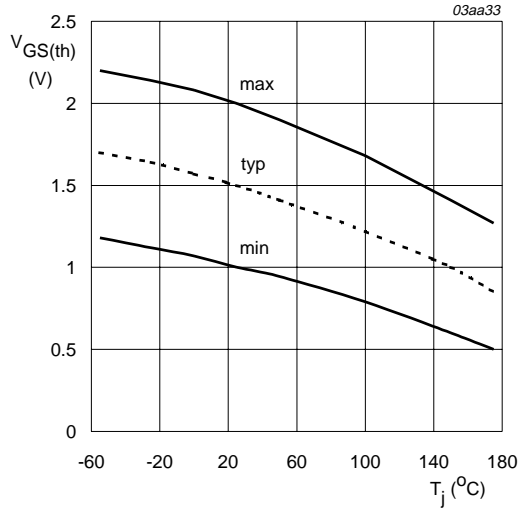
$T_j = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



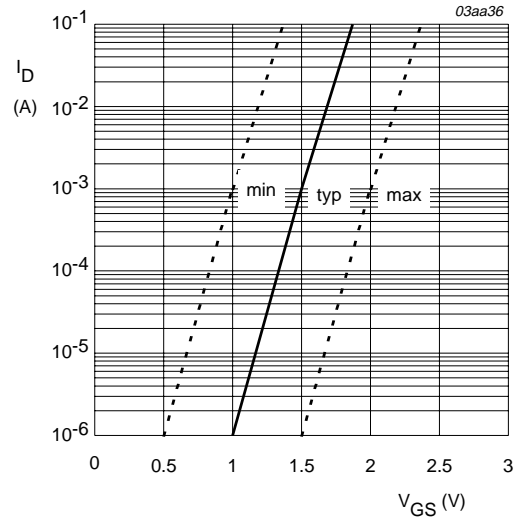
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



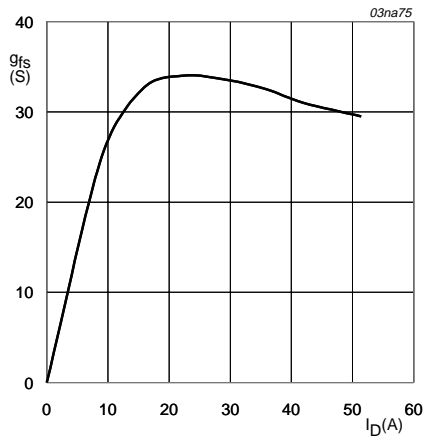
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



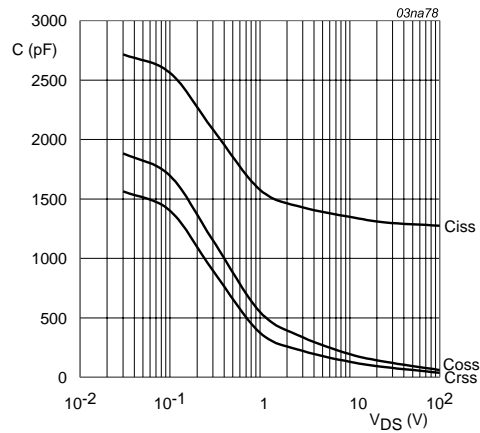
$T_j = 25 \text{ }^{\circ}C; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



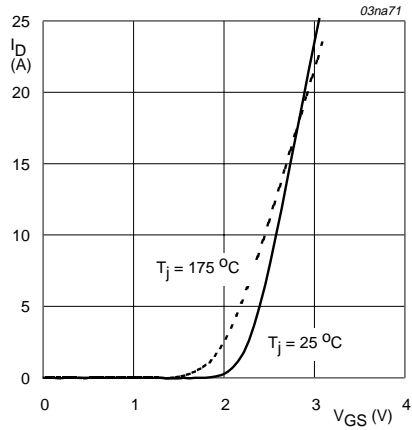
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



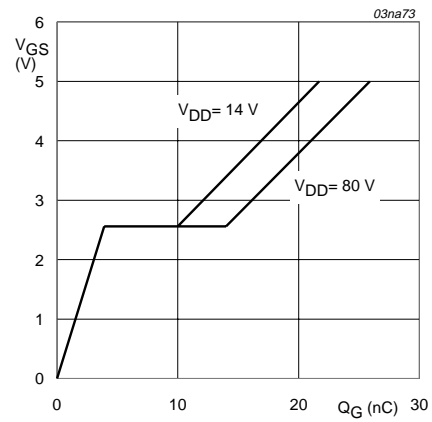
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



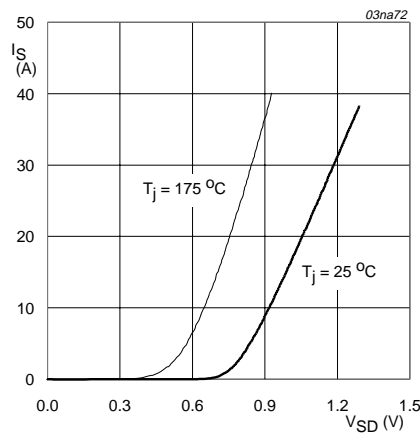
$V_{DS} = 25\text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}; I_D = 20\text{ A}$

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.



$V_{GS} = 0\text{ V}$

Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.

9. Package outline

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads
(one lead cropped)

SOT428

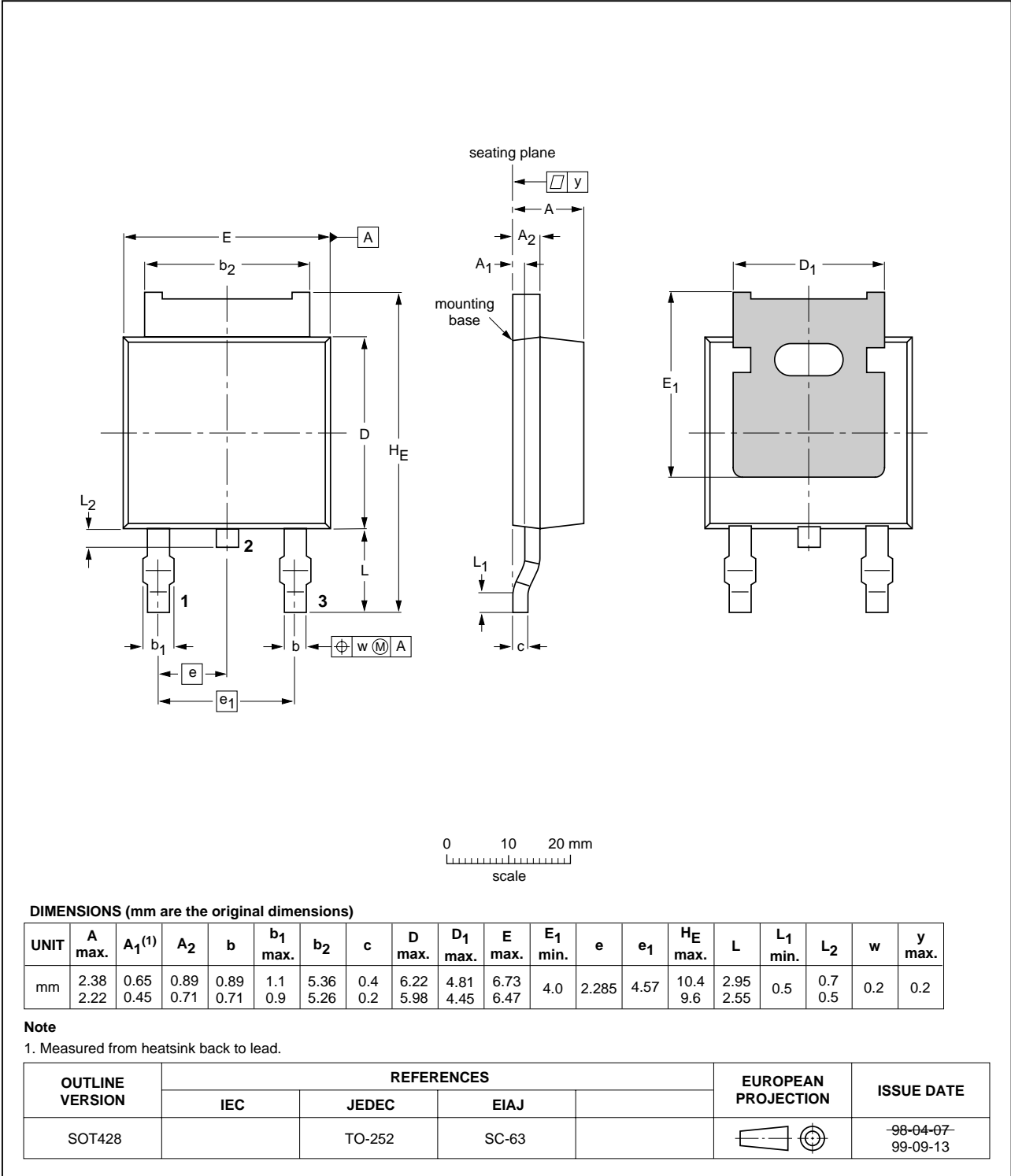


Fig 16. SOT428 (D-PAK).

10. Revision history

Table 6: Revision history

Rev	Date	PCPN	Description
02	20010104	-	Product specification; second version; supersedes Rev. 01 of 20001003. <ul style="list-style-type: none">• Max value of 'W_{DSS}' changed from '14.5 mJ' to '100 mJ' in table 3 "Limiting values"; Value of 'I_D' changed from '17 A' to '14 A' in the 'Conditions' column of 'W_{DSS}'; see Section 6 on page 2.• '42 V' logo added to front page of data sheet.
01	20001003	-	Product specification; initial version.

11. Data sheet status

Datasheet status	Product status	Definition ^[1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Argentina: see South America

Australia: Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Tel. +43 160 101, Fax. +43 160 101 1210

Belarus: Tel. +375 17 220 0733, Fax. +375 17 220 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Tel. +359 268 9211, Fax. +359 268 9102

Canada: Tel. +1 800 234 7381

China/Hong Kong: Tel. +852 2 319 7888, Fax. +852 2 319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Tel. +45 3 288 2636, Fax. +45 3 157 0044

Finland: Tel. +358 961 5800, Fax. +358 96 158 0920

France: Tel. +33 14 099 6161, Fax. +33 14 099 6427

Germany: Tel. +49 40 23 5360, Fax. +49 402 353 6300

Hungary: see Austria

India: Tel. +91 22 493 8541, Fax. +91 22 493 8722

Indonesia: see Singapore

Ireland: Tel. +353 17 64 0000, Fax. +353 17 64 0200

Israel: Tel. +972 36 45 0444, Fax. +972 36 49 1007

Italy: Tel. +39 039 203 6838, Fax. +39 039 203 6800

Japan: Tel. +81 33 740 5130, Fax. +81 3 3740 5057

Korea: Tel. +82 27 09 1412, Fax. +82 27 09 1415

Malaysia: Tel. +60 37 50 5214, Fax. +60 37 57 4880

Mexico: Tel. +9-5 800 234 7381

Middle East: see Italy

For all other countries apply to: Philips Semiconductors,
Marketing Communications,
Building BE, P.O. Box 218, 5600 MD EINDHOVEN,
The Netherlands, Fax. +31 40 272 4825

Netherlands: Tel. +31 40 278 2785, Fax. +31 40 278 8399

New Zealand: Tel. +64 98 49 4160, Fax. +64 98 49 7811

Norway: Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Tel. +63 28 16 6380, Fax. +63 28 17 3474

Poland: Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Tel. +34 33 01 6312, Fax. +34 33 01 4107

Sweden: Tel. +46 86 32 2000, Fax. +46 86 32 2745

Switzerland: Tel. +41 14 88 2686, Fax. +41 14 81 7730

Taiwan: Tel. +886 22 134 2451, Fax. +886 22 134 2874

Thailand: Tel. +66 23 61 7910, Fax. +66 23 98 3447

Turkey: Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: Tel. +381 11 3341 299, Fax. +381 11 3342 553

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(SCA70)

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