PROCESS CP205

Central™ Semiconductor Corp.

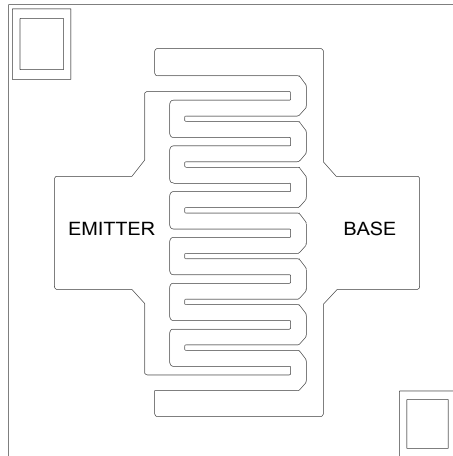
Small Signal Transistors

NPN - Silicon RF Transistor Chip

PROCESS DETAILS

PROCESS	EPITAXIAL PLANAR
DIE SIZE	15 x 15 MILS
DIE THICKNESS	7.5 MILS
BASE BONDING PAD AREA	2.0 x 2.4 MILS
EMITTER BONDING PAD AREA	2.0 x 2.7 MILS
TOP SIDE METALIZATION	Al
BACK SIDE METALIZATION	Au - 16,000Å

GEOMETRY



BACKSIDE COLLECTOR

PRINCIPAL DEVICE TYPES

2N3866

Please refer to selection guide on page 19.

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