PROCESS CP301

Central™ Semiconductor Corp.

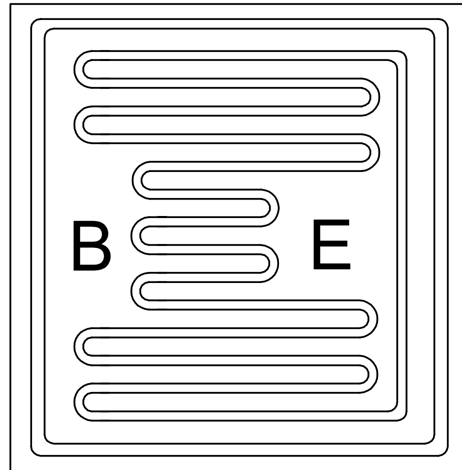
Small Signal Transistors

NPN - High Voltage Transistor Chip

PROCESS DETAILS

PROCESS	EPITAXIAL PLANAR
DIE SIZE	26 x 26 MILS
DIE THICKNESS	9.0 MILS
BASE BONDING PAD AREA	6.1 x 4.9 MILS
EMITTER BONDING PAD AREA	5.2 x 5.2 MILS
TOP SIDE METALIZATION	Al - 30,000Å
BACK SIDE METALIZATION	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR

PRINCIPAL DEVICE TYPES

- 2N3439
- 2N3440
- CMPTA42
- CMPT6517
- CXTA42
- CZTA42
- MPSA42

Please refer to selection guide on page 19.

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