PROCESS CP304

Small Signal Transistor

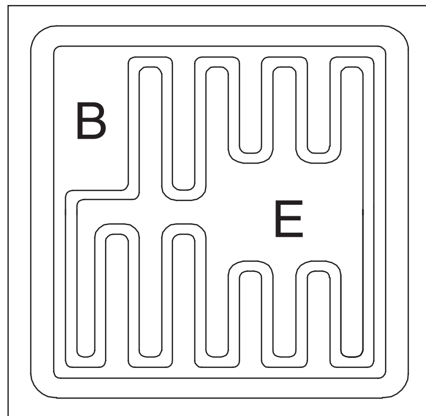
NPN - High Current Transistor Chip

Central™
Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	22 x 22 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	5.7 X 4.0 MILS
Emitter Bonding Pad Area	5.3 X 4.0 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR R0

GROSS DIE PER 4 INCH WAFER
23,450

PRINCIPAL DEVICE TYPES
MPSA05
MPSA06

145 Adams Avenue
Hauppauge, NY 11788 USA
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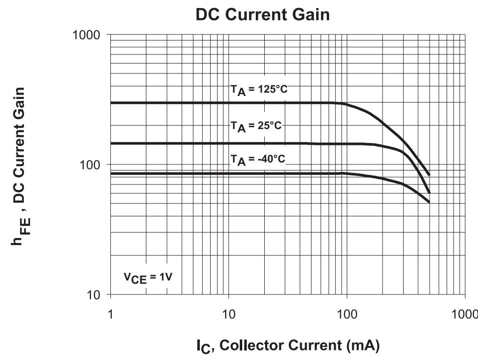
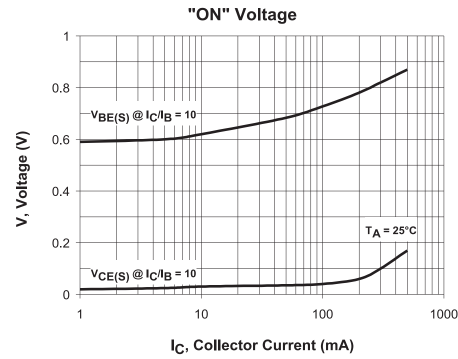
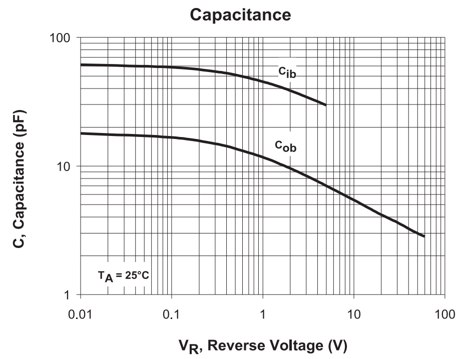
R2 (1-August 2002)

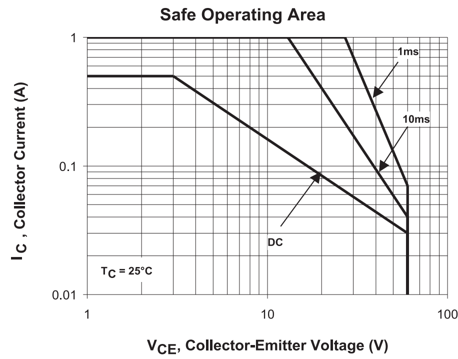
PROCESS CP304

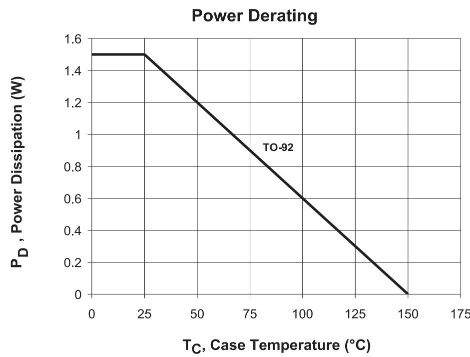
Typical Electrical Characteristics

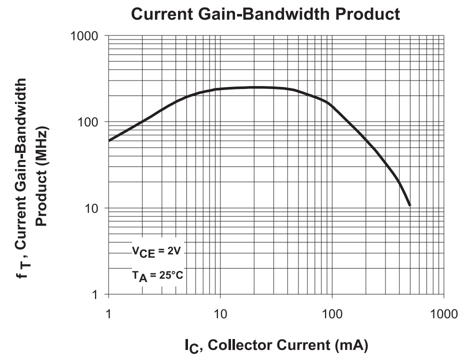












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