

P-Channel NexFET™ Power MOSFET

FEATURES

- Dual P-Ch MOSFETs
- Common Source Configuration
- Small Footprint 1mm × 1.5mm
- Gate-Source Voltage Clamp
- Gate ESD Protection –3kV
- Pb Free
- RoHS Compliant
- Halogen Free

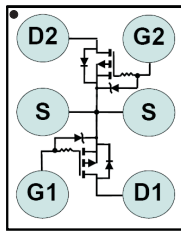
APPLICATIONS

- Battery Management
- Load Switch
- Battery Protection

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile. Low on resistance coupled with the small footprint and low profile make the device ideal for battery operated space constrained applications.

Figure 1. Top View



PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	-20	V
Q_g	Gate Charge Total (-4.5V)	1.6	nC
Q_{gd}	Gate Charge Gate to Drain	0.4	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -1.8V$	145 mΩ
		$V_{GS} = -2.5V$	115 mΩ
		$V_{GS} = -4.5V$	95 mΩ
$R_{D1D2(on)}$	Drain to Drain On Resistance	$V_{GS} = -1.8V$	245 mΩ
		$V_{GS} = -2.5V$	180 mΩ
		$V_{GS} = -4.5V$	140 mΩ
$V_{GS(th)}$	Threshold Voltage	-0.65	V

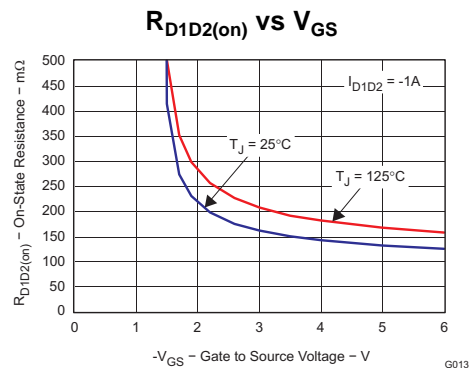
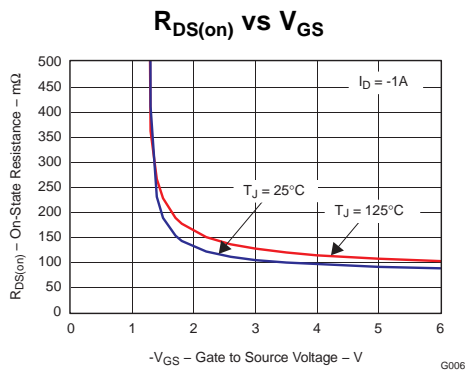
ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD75205W1015	1-mm × 1.5-mm Wafer Level Package	7-Inch Reel	3000	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	-6	V
I_{DS}	Continuous Drain to Source Current, $T_C = 25^\circ\text{C}^{(1)}$	-1.2	A
	Pulsed Drain to Source Current, $T_C = 25^\circ\text{C}^{(2)}$	-9.6	A
I_S	Continuous Source Pin Current	-2.3	A
	Pulsed Source Pin Current ⁽²⁾	-30	A
I_G	Continuous Gate Clamp Current	-0.5	A
	Pulsed Gate Clamp Current ⁽²⁾	-7	A
P_D	Power Dissipation ⁽¹⁾	0.75	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

- (1) Per device, both sides in conduction
 (2) Pulse duration 10μs, duty cycle ≤2%



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Static Characteristics							
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_{DS} = -250\mu A$	-20			V	
BV_{GSS}	Gate to Source Voltage	$V_{DS} = 0V, I_G = -250\mu A$	-6.1		-7.2	V	
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = -16V$			-1	μA	
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = -6V$			-100	nA	
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = -250\mu A$	-0.45	-0.65	-0.85	V	
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -1.8V, I_D = -1A$		145	180	m Ω	
		$V_{GS} = -2.5V, I_D = -1A$		115	145	m Ω	
		$V_{GS} = -4.5V, I_D = -1A$		95	120	m Ω	
$R_{D1D2(on)}$	Source to Drain On Resistance	$V_{GS} = -1.8V, I_{D1D2} = -1A$		245	305	m Ω	
		$V_{GS} = -2.5V, I_{D1D2} = -1A$		180	225	m Ω	
		$V_{GS} = -4.5V, I_{D1D2} = -1A$		140	175	m Ω	
g_{fs}	Transconductance	$V_{DS} = -10V, I_D = -1A$		5		S	
Dynamic Characteristics							
C_{ISS}	Input Capacitance	$V_{GS} = 0V, V_{DS} = -10V,$ $f = 1MHz$		205	265	pF	
C_{OSS}	Output Capacitance			80	105	pF	
C_{RSS}	Reverse Transfer Capacitance			25	33	pF	
Q_g	Gate Charge Total (-4.5V)			1.6	2.2	nC	
Q_{gd}	Gate Charge - Gate to Drain		$V_{DS} = -10V,$ $I_{DS} = -1A$		0.4		nC
Q_{gs}	Gate Charge - Gate to Source				0.3		nC
$Q_{g(th)}$	Gate Charge at V_{th}				0.12		nC
Q_{OSS}	Output Charge	$V_{DS} = -10.25V, V_{GS} = 0V$		1.5		nC	
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = -10V, V_{GS} = -4.5V,$ $I_{DS} = -1A, R_G = 10\Omega$		6.3		ns	
t_r	Rise Time			5.3		ns	
$t_{d(off)}$	Turn Off Delay Time			32		ns	
t_f	Fall Time			17		ns	
Diode Characteristics							
V_{SD}	Diode Forward Voltage	$I_{DS} = -1A, V_{GS} = 0V$	-0.75		-1	V	
Q_{rr}	Reverse Recovery Charge	$V_{dd} = -10.25V, I_F = -1A, di/dt = 200A/\mu s$		5.7		nC	
t_{rr}	Reverse Recovery Time	$V_{dd} = -10.25V, I_F = -1A, di/dt = 200A/\mu s$		15.7		ns	

THERMAL CHARACTERISTICS

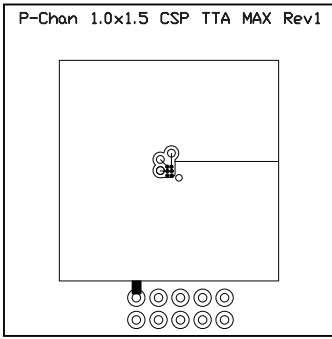
$T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^{(1) (2)}			212	$^\circ\text{C}/\text{W}$
	Thermal Resistance Junction to Ambient ^{(2) (3)}			119	$^\circ\text{C}/\text{W}$

(1) Device mounted on FR4 material with Minimum Cu mounting area

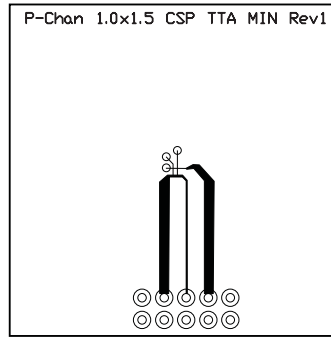
(2) Measured with both devices biased in a parallel condition.

(3) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



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Max $R_{\theta JA} = 119^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of 2-
oz. (0.071-mm thick)
Cu.

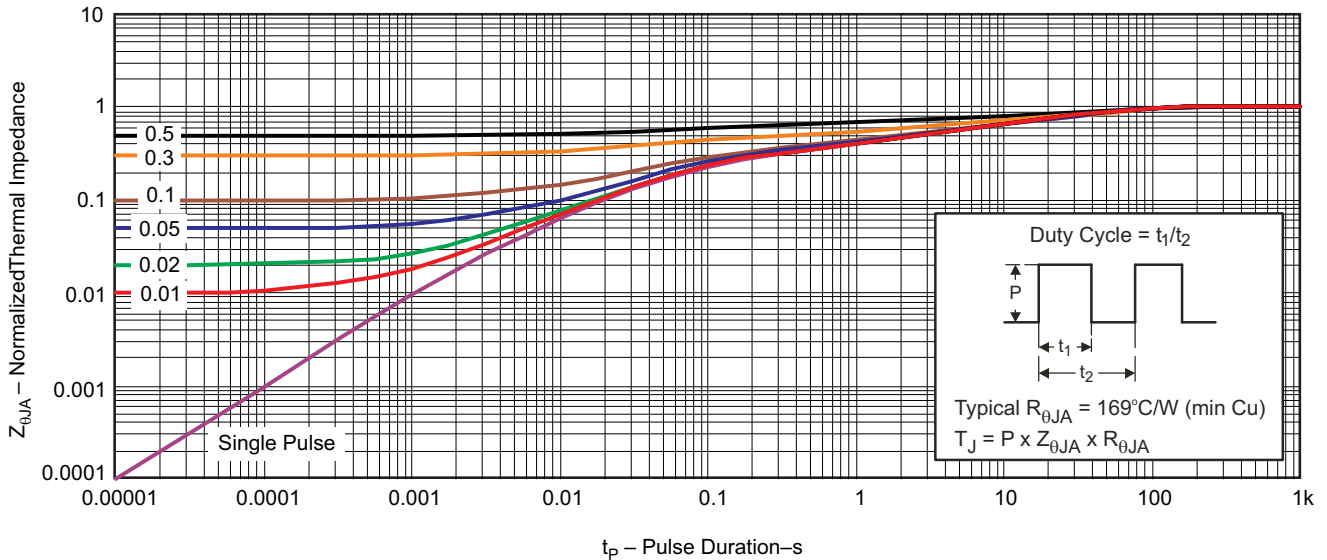


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Max $R_{\theta JA} = 212^{\circ}\text{C/W}$
when mounted on
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

Graphs are Per MOSFET at $T_A = 25^{\circ}\text{C}$, unless stated otherwise. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).



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Figure 2. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

Graphs are Per MOSFET at $T_A = 25^\circ\text{C}$, unless stated otherwise. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).

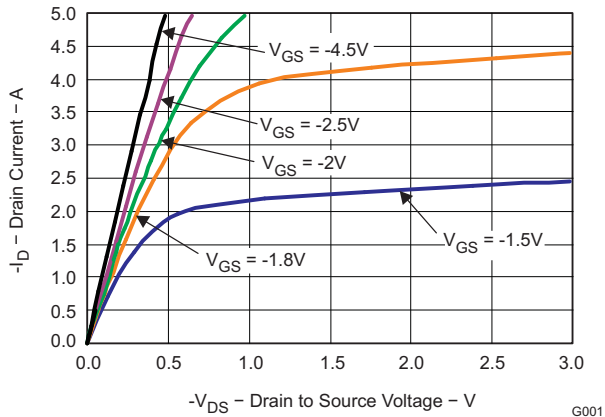


Figure 3. Saturation Characteristics

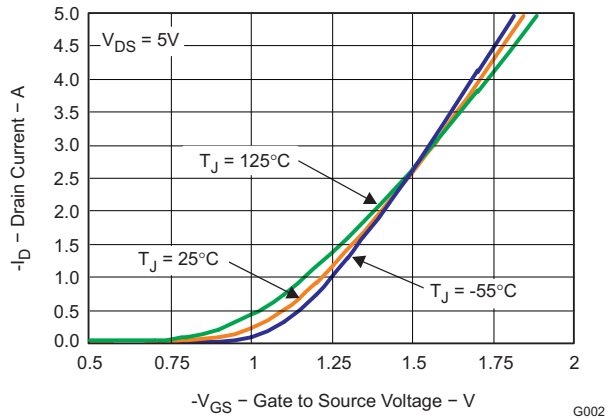


Figure 4. Transfer Characteristics

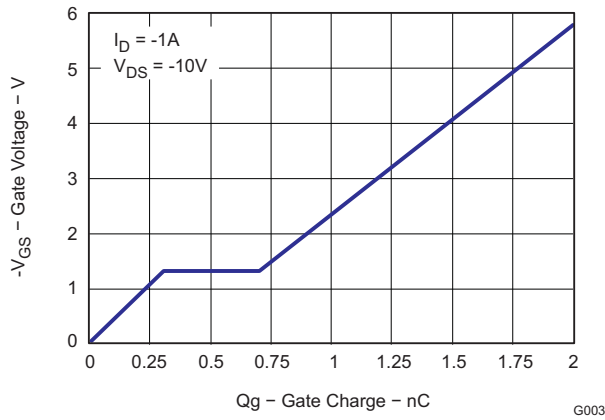


Figure 5. Gate Charge

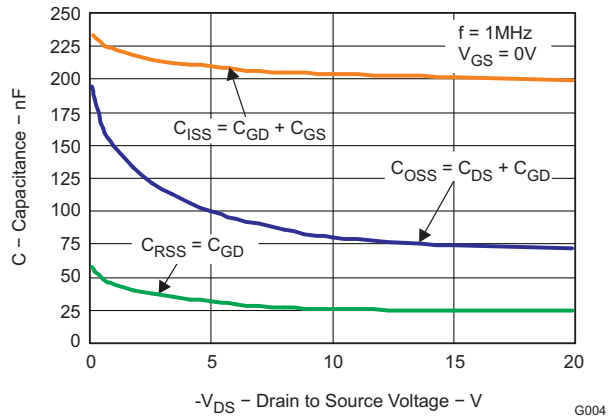


Figure 6. Capacitance

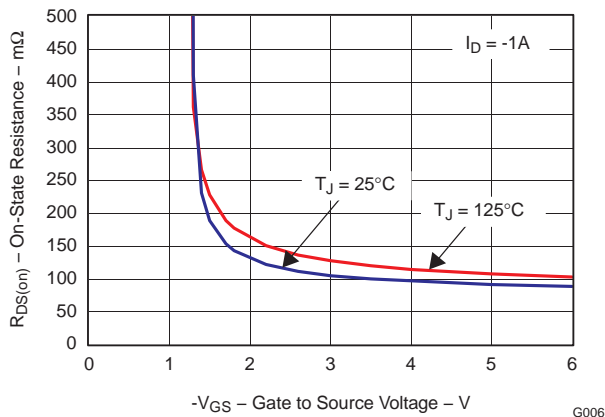


Figure 7. On-State Resistance vs. Gate Voltage

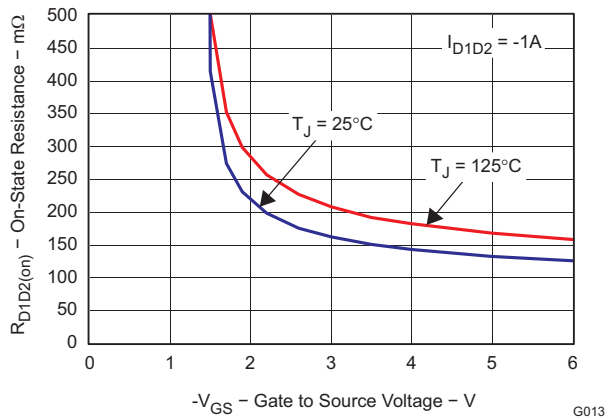


Figure 8. On-State Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

Graphs are Per MOSFET at $T_A = 25^\circ\text{C}$, unless stated otherwise. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).

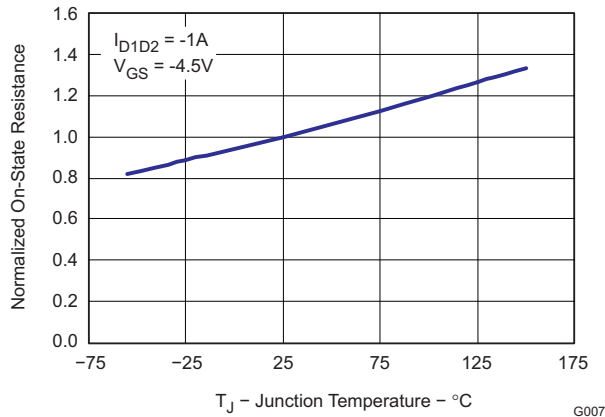


Figure 9. Normalized On-State Resistance vs. Temperature

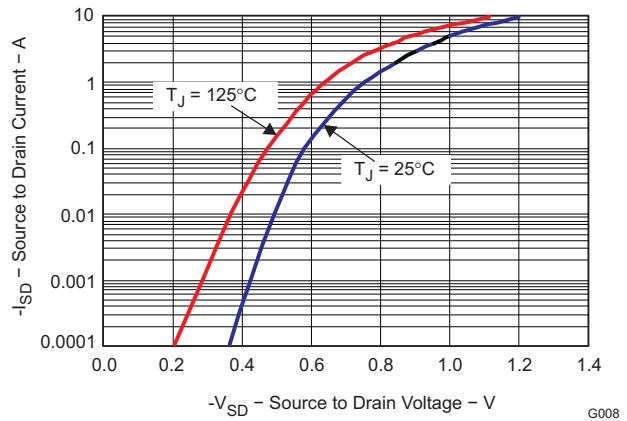


Figure 10. Typical Diode Forward Voltage

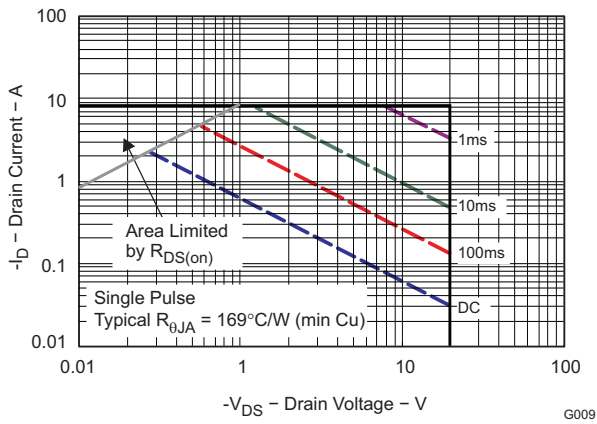


Figure 11. Maximum Safe Operating Area

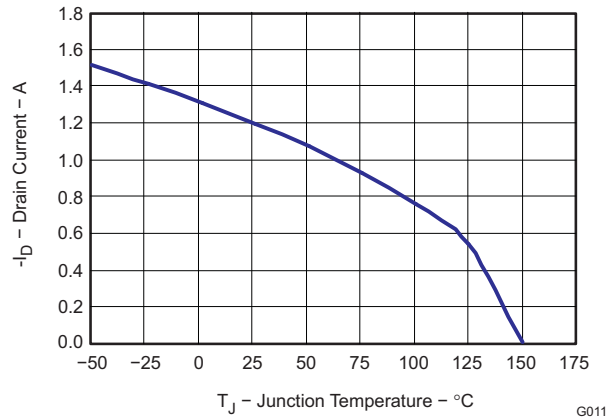


Figure 12. Maximum Drain Current vs. Temperature

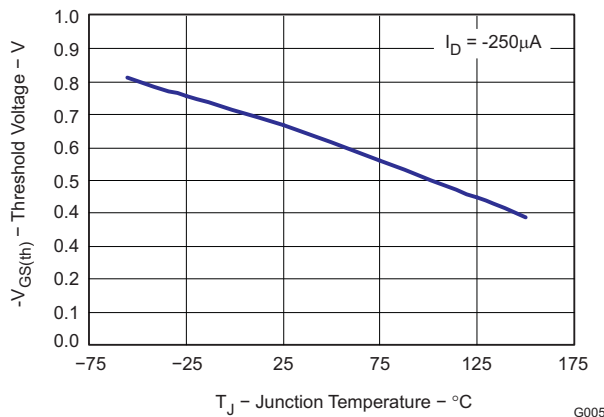
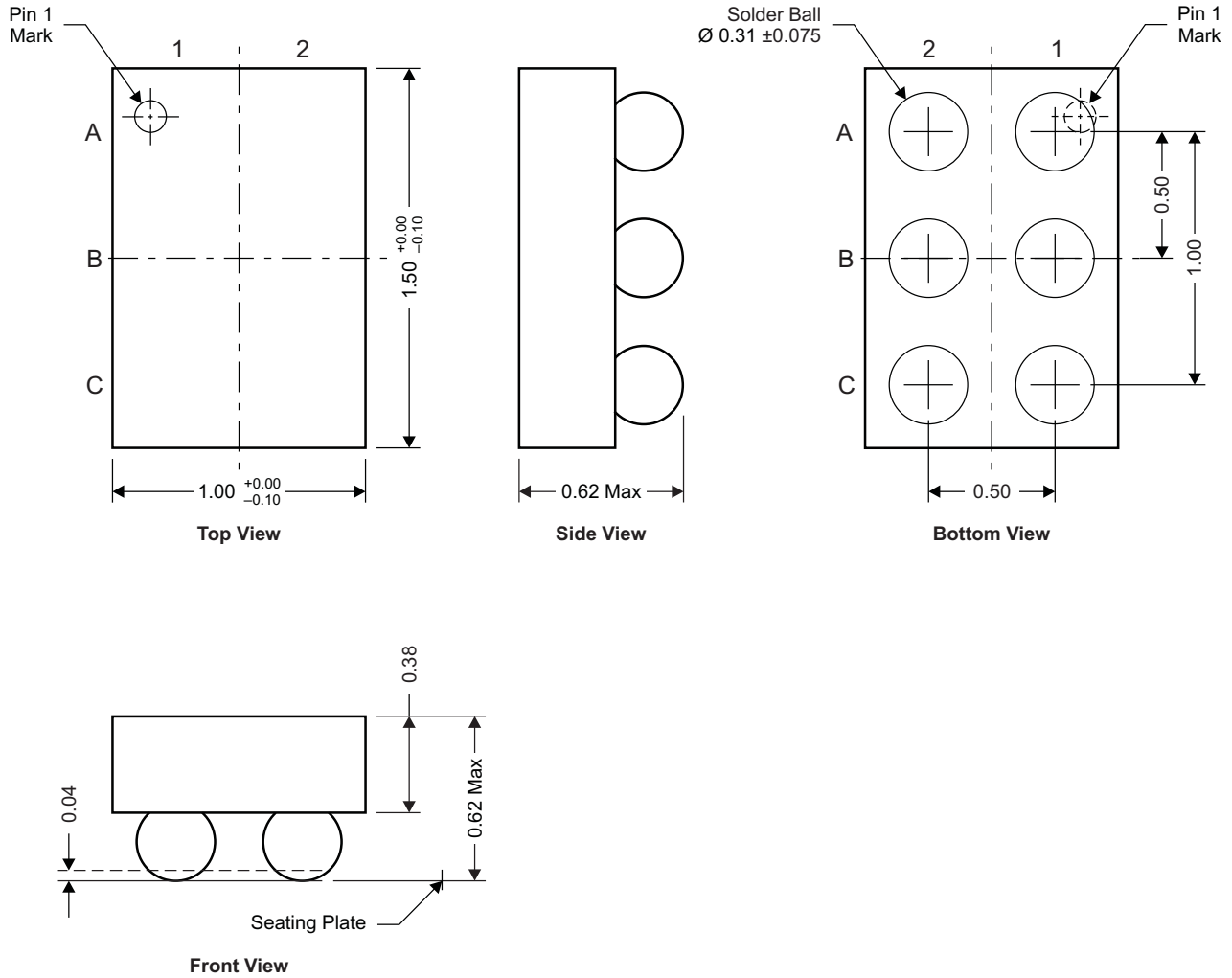


Figure 13. Threshold Voltage vs. Temperature

MECHANICAL DATA

CSD75205W1015 Package Dimensions



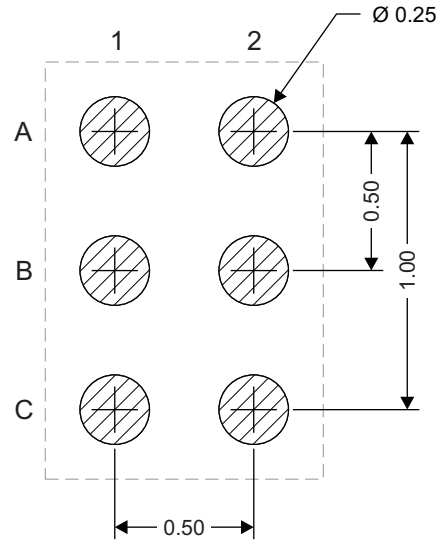
NOTE: All dimensions are in mm (unless otherwise specified)

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Pinout

POSITION	DESIGNATION
B1, B2	Source
C1	Gate1
C2	Drain1
A2	Gate2
A1	Drain2

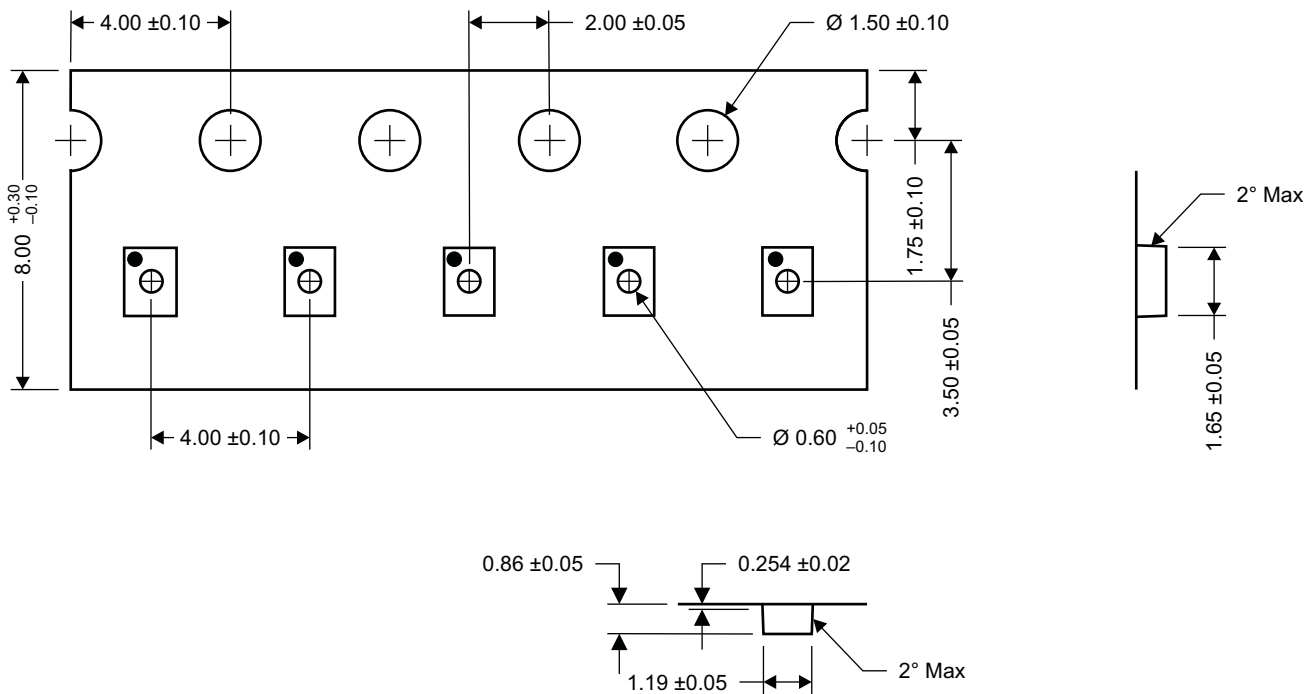
Figure 14. Land Pattern Recommendation



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NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



M0159-01

NOTE: All dimensions are in mm (unless otherwise specified)

REVISION HISTORY

Changes from Original (October 2009) to Revision A **Page**

- Deleted the Package Marking Information section [7](#)
-

Changes from Revision A (October 2009) to Revision B **Page**

- Changed the CSD75205W1015 Package Dimensions section. Top View From: 15.00 To: 1.50 [6](#)
-

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