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U.S.A.

PNP POWER TRANSISTORS

COMPLEMENTARY TO THE D40D SERIES

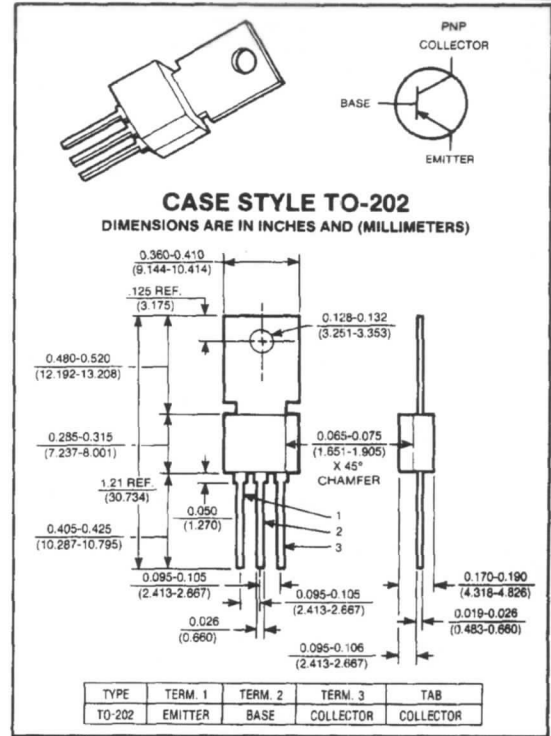
D41D Series

-30 - -60 VOLTS
-1 AMP, 6.25 WATTS

D41D is a power transistor designed for various specific and general purpose applications, such as: output and driver stages of amplifiers operating at frequencies from DC to greater than 1.0 MHz; series, shunt and switching regulators; low and high frequency inverters/converters; and many others.

Features:

- High free-air power dissipation
- PNP complement to D40D NPN
- Low collector saturation voltage (-0.5V typ. @ 1.0A I_C)
- Excellent linearity
- Fast Switching



maximum ratings ($T_A = 25^\circ C$) (unless otherwise specified)

RATING	SYMBOL	D41D1, 2	D41D4, 5	D41D7, 8	UNITS
Collector-Emitter Voltage	V_{CEO}	-30	-45	-60	Volts
Collector-Emitter Voltage	V_{CES}	-45	-60	-75	Volts
Emitter Base Voltage	V_{EBO}	-5	-5	-5	Volts
Collector Current — Continuous	I_C	-1	-1	-1	A
Peak ⁽¹⁾	I_{CM}	-1.5	-1.5	-1.5	A
Base Current — Continuous	I_B	-5	-5	-5	A
Total Power Dissipation @ $T_A = 25^\circ C$ @ $T_C = 25^\circ C$	P_D	1.67 6.25	1.67 6.25	1.67 6.25	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	-55 to +150	-55 to +150	$^\circ C$

thermal characteristics

Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	75	75	$^\circ C/W$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	20	20	20	$^\circ C/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	+260	+260	+260	$^\circ C$

(1) Pulse Test Pulse Width = 300ms Duty Cycle \leq 2%.

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electrical characteristics ($T_C = 25^\circ C$) (unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
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off characteristics⁽¹⁾

Collector-Emitter Sustaining Voltage ($I_C = 10mA$)	D41D1, 2 D41D4, 5 D41D7, 8	$V_{CEO(sus)}$	-30 -45 -60	— — —	— — —	Volts
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEO}$) ($V_{CE} = \text{Rated } V_{CES}$)	$T_C = 25^\circ C$ $T_C = 150^\circ C$	I_{CES}	— —	— -1	-0.1 —	μA
Emitter Cutoff Current ($V_{EB} = 5V$)		I_{EBO}	—	—	-0.1	μA

second breakdown

Second Breakdown with Base Forward Biased	FBSOA	SEE FIGURE 7
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on characteristics

DC Current Gain ($I_C = 100mA, V_{CE} = 2V$)	D41D1, 4, 7 D41D2, 5, 8	h_{FE}	50 120	— —	150 360	—
($I_C = 1A, V_{CE} = 2V$)	D41D1, 4, 7 D41D2 D41D5, 8	h_{FE}	10 20 10	— — —	— — —	—
Collector-Emitter Saturation Voltage ($I_C = -500mA, I_B = -50mA$)	D41D1, 2, 4, 5 D41D7, 8	$V_{CE(sat)}$	— —	— —	0.5 1.0	Volts
Base-Emitter Saturation Voltage ($I_C = -500mA, I_B = -50mA$)		$V_{BE(sat)}$	—	—	1.5	Volts

dynamic characteristics

Collector Capacitance ($V_{CB} = 10V, f = 1MHz$)	C_{CBO}	—	10	—	μF
Current-Gain — Bandwidth Product ($I_C = -20mA, V_{CE} = -10V$)	f_T	—	150	—	MHz

switching characteristics

Resistive Load								
Delay Time + Rise Time	$I_C = -1A, I_{B1} = I_{B2} = -0.1A$	$t_d + t_r$	—	50	—			
Storage Time						t_s	—	75
Fall Time								
		$V_{CC} = -30V, t_p = 25 \mu sec$						

(1) Pulse Test PW = 300ms Duty Cycle \leq 2%.

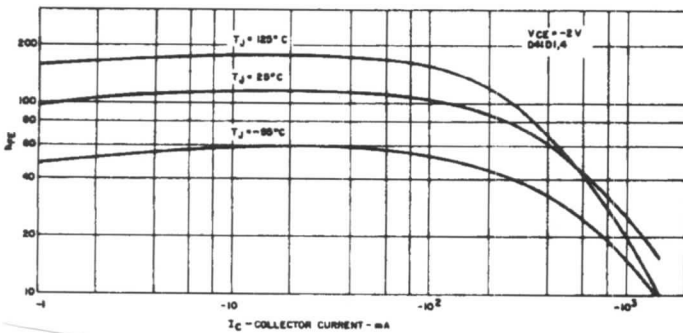


FIG. 1

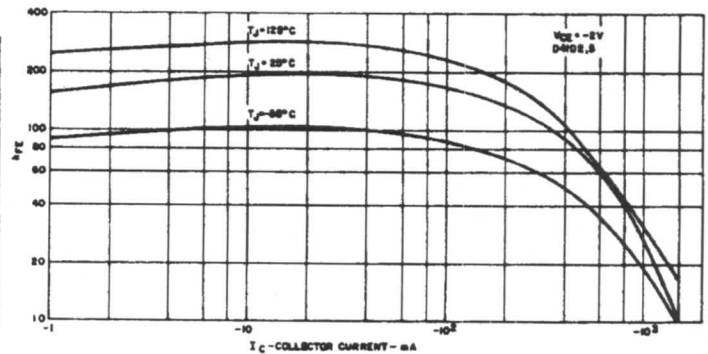


FIG. 2

TYPICAL h_{FE} VS. I_C