FAIRCHILD SEMICONDUCTOR®

February 2012

UniFET-II™

FDD5N50NZF

N-Channel MOSFET

500V, 3.7A, 1.75Ω

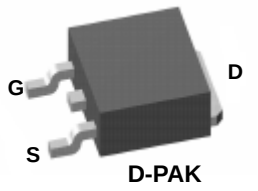
Features

- $R_{DS(on)}$ = 1.47Ω (Typ.)@ V_{GS} = 10V, I_D = 1.85A
- Low Gate Charge (Typ. 9nC)
- Low C_{rss} (Typ. 4pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Imoroved Capability
- RoHS Compliant

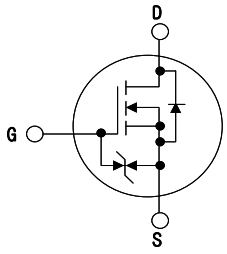
Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advance technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switching mode power supplies and active power factor correction.



D-PAK



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter			FDD5N50NZF	Units
V_{DSS}	Drain to Source Voltage			500	V
V_{GSS}	Gate to Source Voltage			±25	V
I_D	Drain Current	-Continuous (T_C = 25°C)		3.7	A
		-Continuous (T_C = 100°C)		2.2	
I_{DM}	Drain Current	- Pulsed	(Note 1)	14	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	165	mJ
I_{AR}	Avalanche Current		(Note 1)	3.3	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	6.25	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	20	V/ns
P_D	Power Dissipation	(T_C = 25°C)		62.5	W
		- Derate above 25°C		0.5	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300	°C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDD5N50NZF	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD5N50NZF	FDD5N50NZFTM	D-PAK	380mm	16mm	2500

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V, $T_C = 25^oC$	500	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25^oC	-	0.5	-	$V/^oC$
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500V, V_{GS} = 0V	-	-	10	μA
		V_{DS} = 400V, V_{GS} = 0V, $T_C = 125^oC$	-	-	100	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±25V, V_{DS} = 0V	-	-	±10	μA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 1.85A	-	1.47	1.75	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20V, I_D = 1.85A (Note 4)	-	4.2	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	365	485	pF
C_{oss}	Output Capacitance		-	50	65	pF
C_{rss}	Reverse Transfer Capacitance		-	4	8	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 400V I_D = 3.7A, V_{GS} = 10V (Note 4, 5)	-	9	12	nC
Q_{gs}	Gate to Source Gate Charge		-	2	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	4	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250V, I_D = 3.7A, V_{GS} = 10V, R_{GEN} = 25Ω (Note 4, 5)	-	12	35	ns
t_r	Turn-On Rise Time		-	19	50	ns
$t_{d(off)}$	Turn-Off Delay Time		-	31	70	ns
t_f	Turn-Off Fall Time		-	22	55	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	3.7	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	14	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_{SD} = 3.7A	-	-	1.5	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_{SD} = 3.7A, dI_F/dt = 100A/μs (Note 4)	-	87	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.15	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 23mH, I_{AS} = 3.7A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. $I_{SD} \le$ 3.7A, di/dt ≤ 200A/μs, $V_{DD} \le BV_{DSS}$, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Dual Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

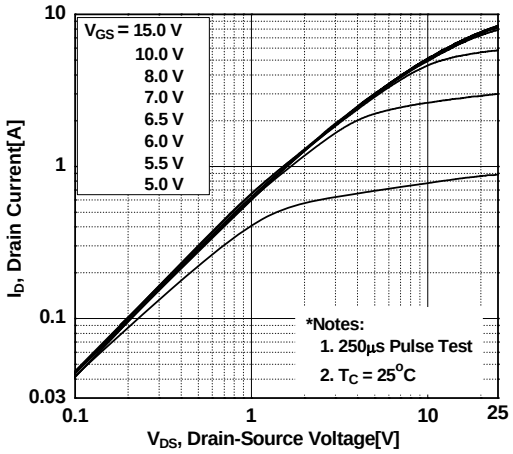


Figure 2. Transfer Characteristics

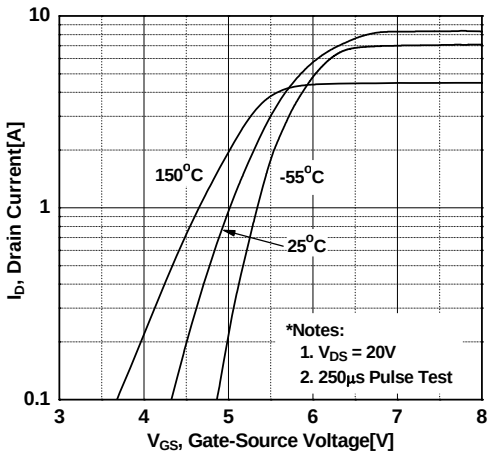


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

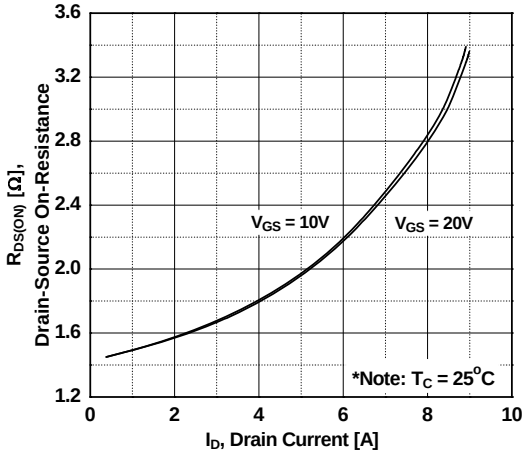


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

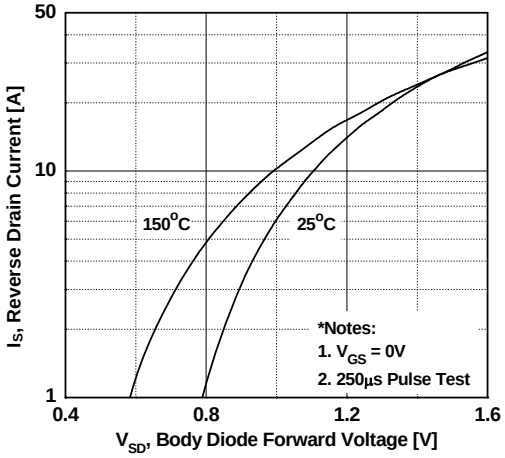


Figure 5. Capacitance Characteristics

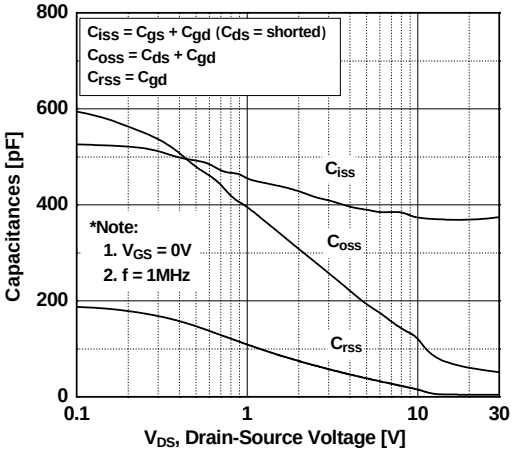
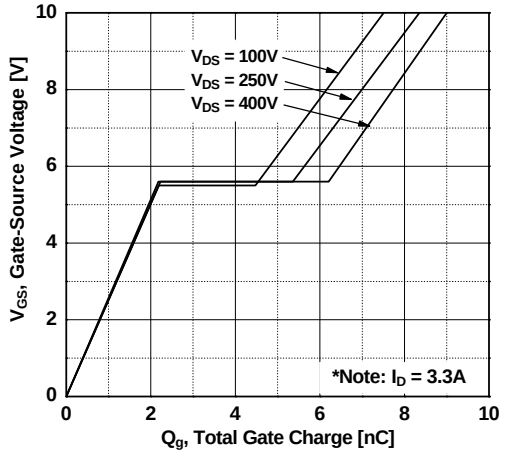


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

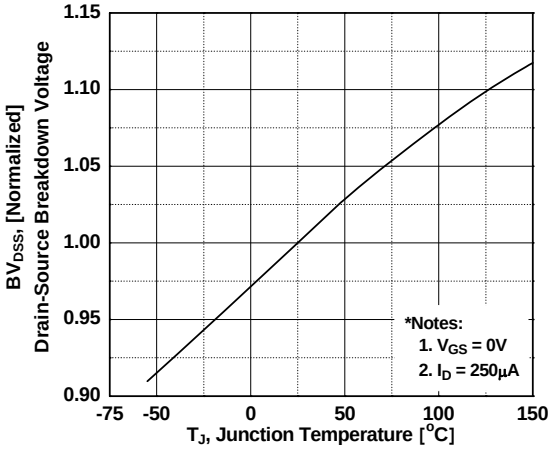


Figure 9. Maximum Safe Operating Area vs. Case Temperature

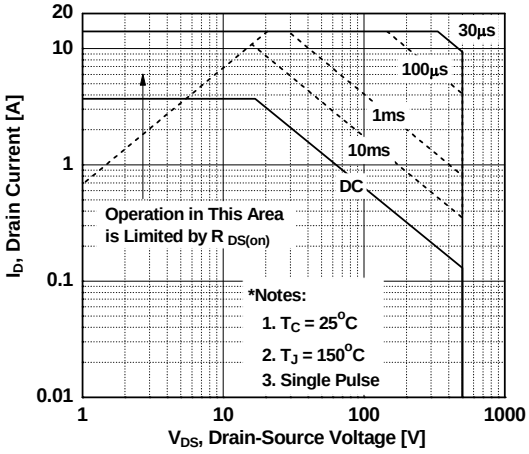


Figure 10. Maximum Drain Current

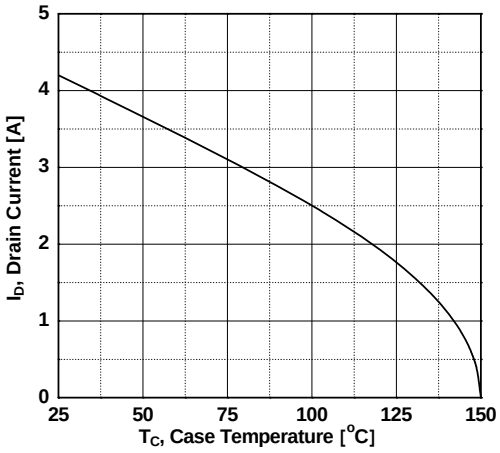
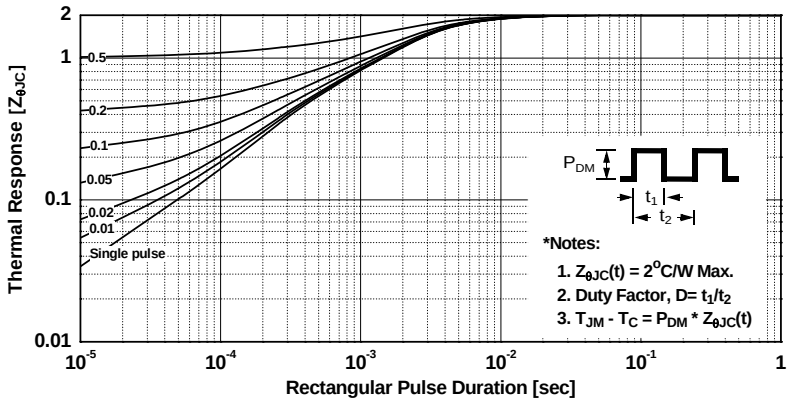
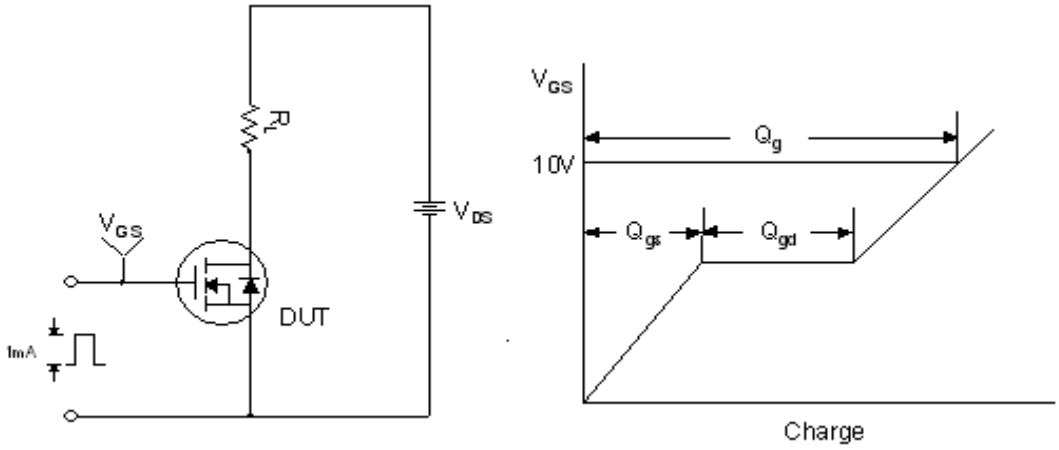


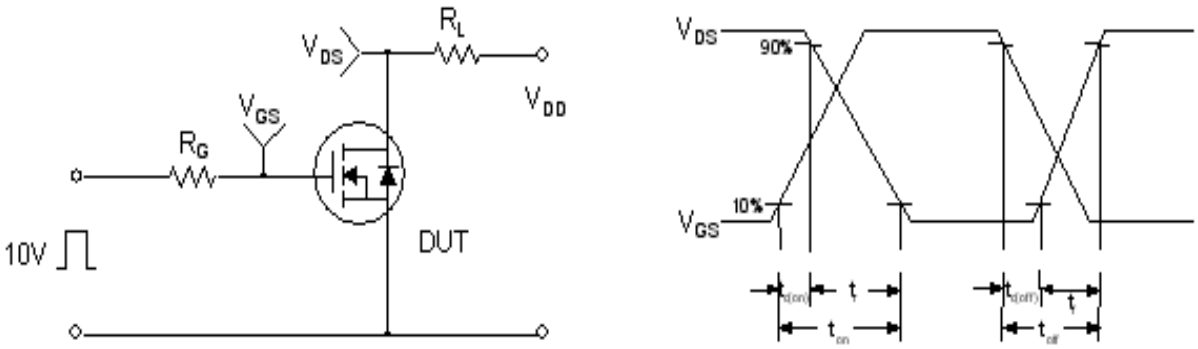
Figure 11. Transient Thermal Response Curve



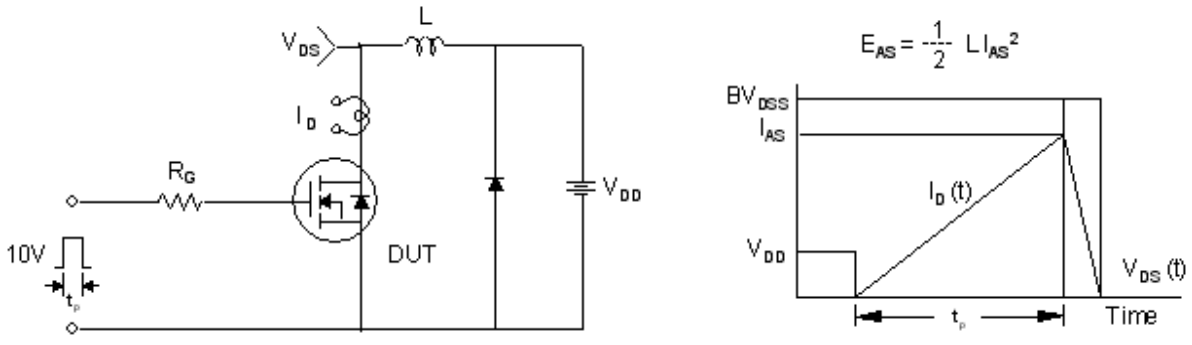
Gate Charge Test Circuit & Waveform



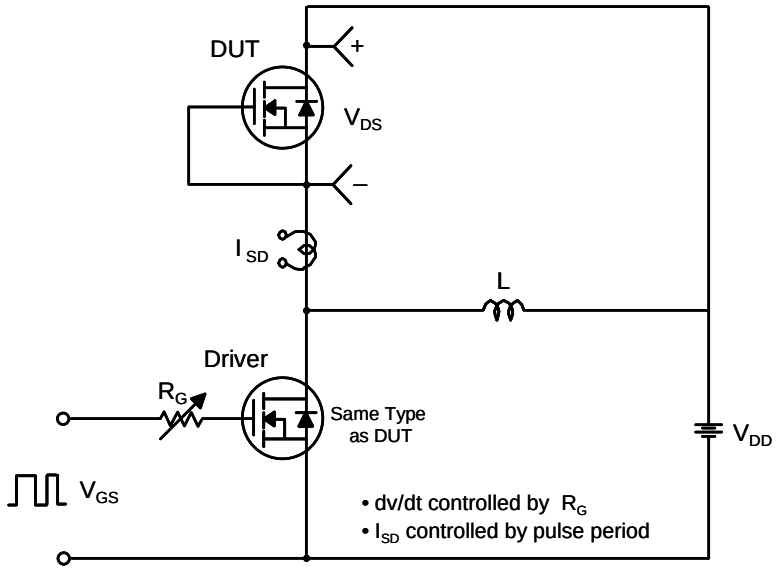
Resistive Switching Test Circuit & Waveforms

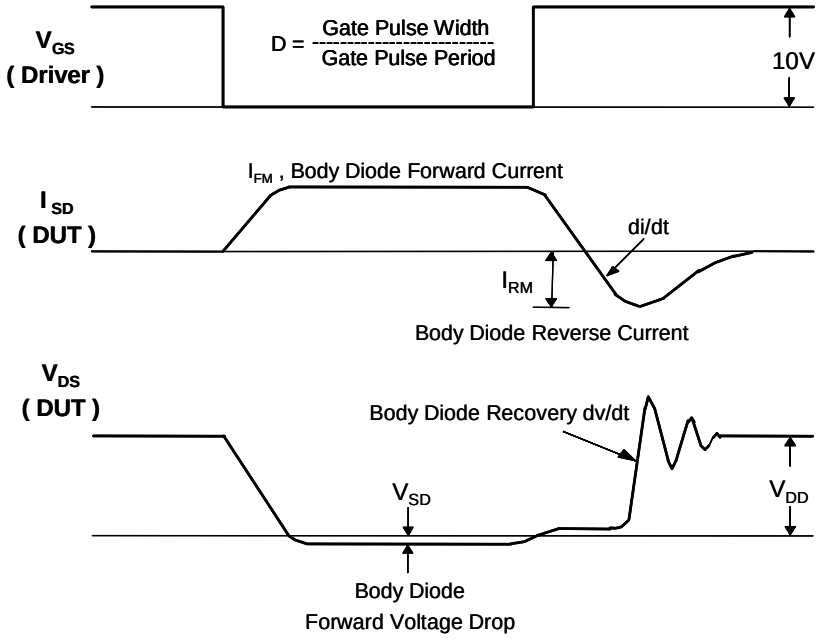


Unclamped Inductive Switching Test Circuit & Waveforms



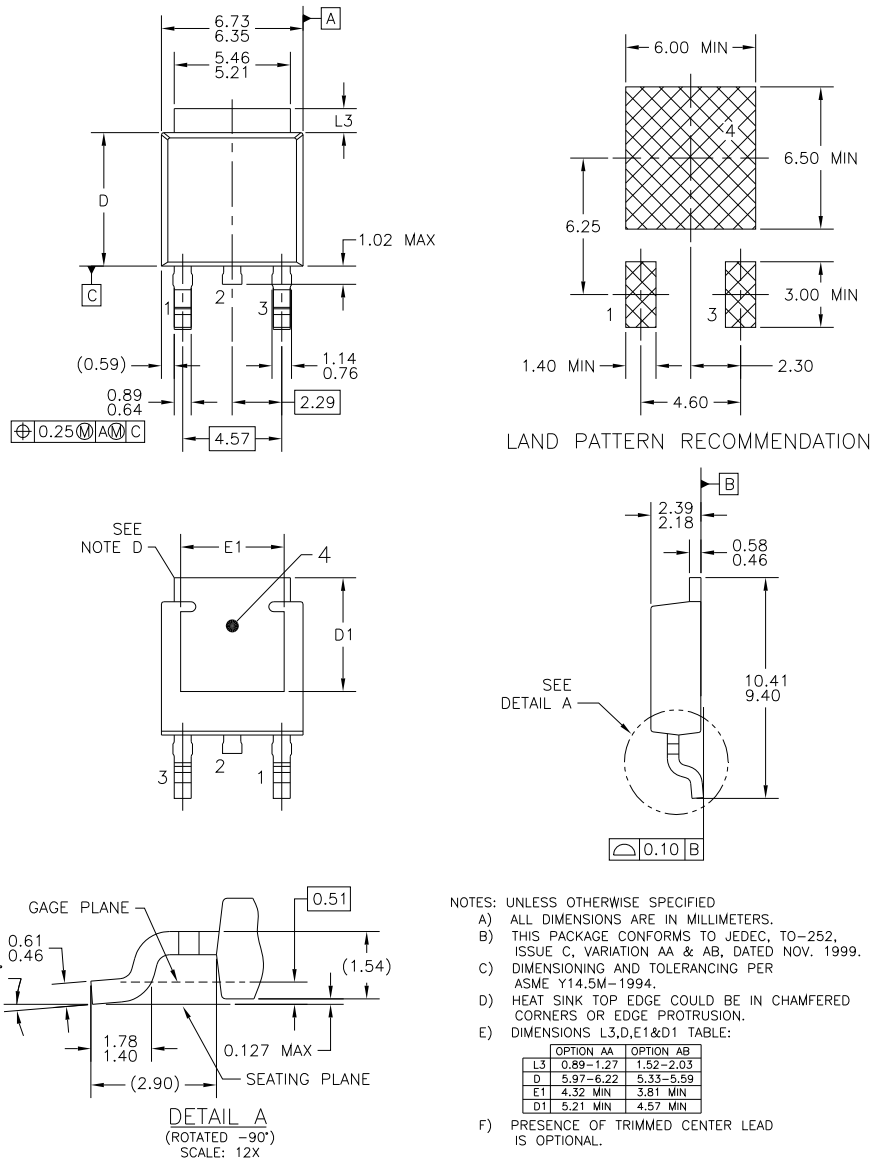
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Mechanical Dimensions

D-PAK



NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.

B) THIS PACKAGE CONFORMS TO JEDEC, TO−252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.

E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION AA	OPTION AB
L3	0.89−1.27	1.52−2.03
D	5.97−6.22	5.33−5.59
E1	4.32 MIN	3.81 MIN
D1	5.21 MIN	4.57 MIN

F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I61