FAIRCHILD

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FDD6682/FDU6682

30V N-Channel PowerTrench$^{\text{®}}$ MOSFET

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

Features

- 75 A, 30 V $R_{DS(ON)}$ = 6.2 mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 8.0 mΩ @ V_{GS} = 4.5 V

- Low gate charge

- Fast switching

- High performance trench technology for extremely low $R_{DS(ON)}$

Applications

- DC/DC converter
- Motor Drives

D-PAK (TO-252)

I-PAK (TO-251AA)

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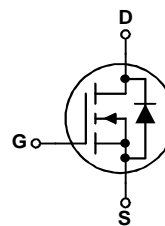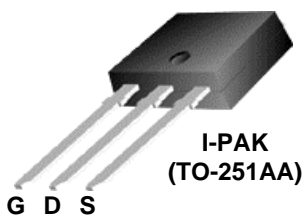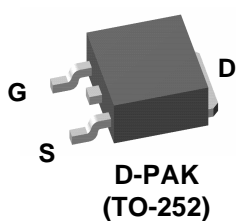
Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	
I_D	Drain Current – Continuous	(Note 3)	75	A
	– Pulsed	(Note 1a)	100	
P_D	Power Dissipation for Single Operation	(Note 1)	71	W
		(Note 1a)	3.8	
		(Note 1b)	1.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	2.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	40	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	96	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape width	Quantity
FDD6682	FDD6682	D-PAK (TO-252)	13''	12mm	2500 units
FDU6682	FDU6682	I-PAK (TO-251)	Tube	N/A	75

Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 2)						
W_{DSS}	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 15$ V, $I_D = 17$ A			240	mJ
I_{AR}	Drain-Source Avalanche Current				17	A
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ µA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C		20		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24$ V, $V_{GS} = 0$ V			1	µA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm20$ V, $V_{DS} = 0$ V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ µA	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C		–7		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10$ V, $I_D = 17$ A $V_{GS} = 4.5$ V, $I_D = 15$ A $V_{GS} = 10$ V, $I_D = 17$ A, $T_J = 125°C$		5.2 6.4 8.0	6.2 8 11.9	mΩ
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10$ V, $V_{DS} = 5$ V	50			A
g_{FS}	Forward Transconductance	$V_{DS} = 5$ V, $I_D = 17$ A		65		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$ V, $f = 1.0$ MHz		2400		pF
C_{oss}	Output Capacitance			577		pF
C_{rss}	Reverse Transfer Capacitance			258		pF
R_G	Gate Resistance	$V_{GS} = 15$ mV, $f = 1.0$ MHz		1.4		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15$ V, $I_D = 1$ A, $V_{GS} = 10$ V, $R_{GEN} = 6$ Ω		14	20	ns
t_r	Turn–On Rise Time			12	37	ns
$t_{d(off)}$	Turn–Off Delay Time			38	64	ns
t_f	Turn–Off Fall Time			18	32	ns
Q_g	Total Gate Charge	$V_{DS} = 15$V, $I_D = 17$ A, $V_{GS} = 5$ V		24	31	nC
Q_{gs}	Gate–Source Charge			6.5		nC
Q_{gd}	Gate–Drain Charge			8.1		nC

Electrical Characteristics (continued) T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				3.2	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 3.2 A (Note 2)		0.7	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 17 A, d_{iF}/d_t = 100 A/µs		32		nS
Q_{rr}	Diode Reverse Recovery Charge			20		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
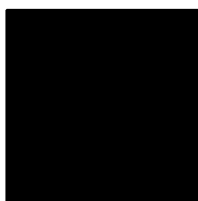
a) $R_{\theta JA}$ = 40°C/W when mounted on a 1in^2 pad of 2 oz copper

b) $R_{\theta JA}$ = 96°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\dfrac{P_D}{R_{DS(ON)}}}$

where P_D is maximum power dissipation at T_C = 25°C and $R_{DS(on)}$ is at $T_{J(max)}$ and V_{GS} = 10V. Package current limitation is 21A
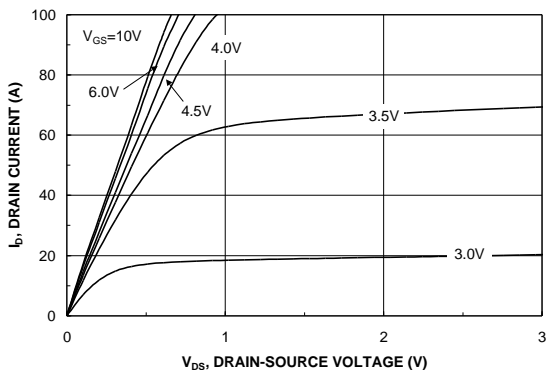
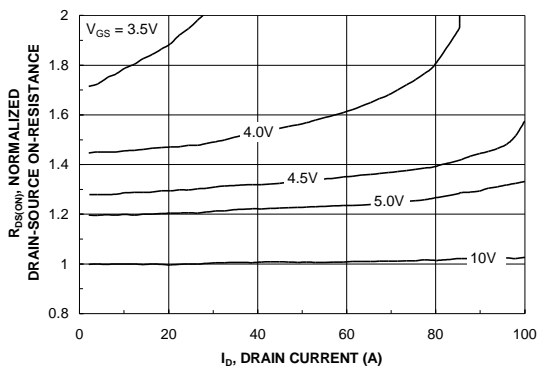# Typical Characteristics

Figure 1. On-Region Characteristics.

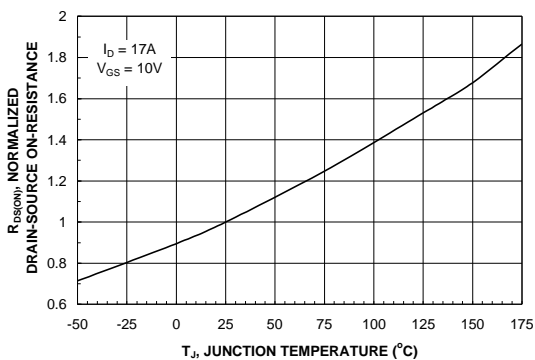**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

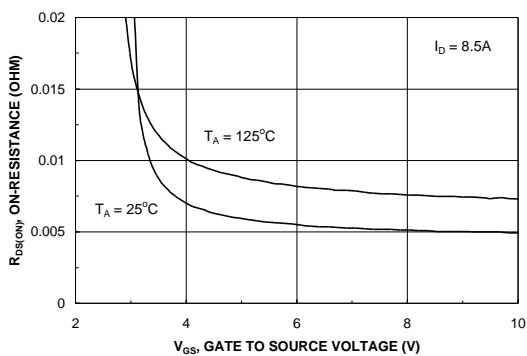**Figure 3. On-Resistance Variation with Temperature.**

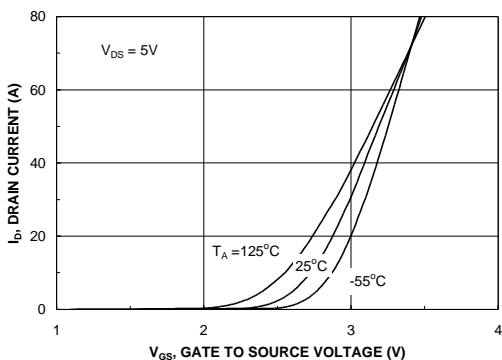**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

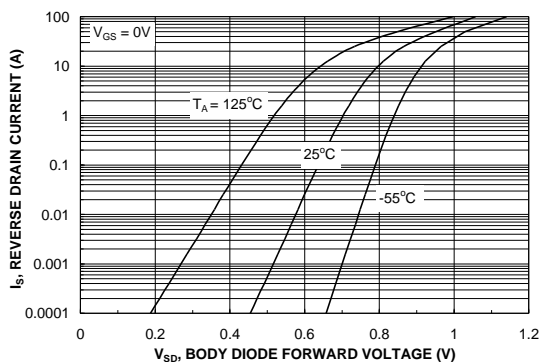**Figure 5. Transfer Characteristics**

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature
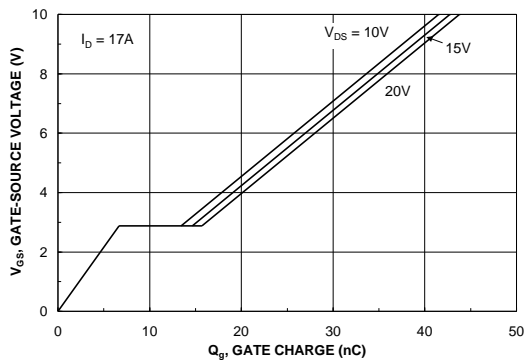
Typical Characteristics
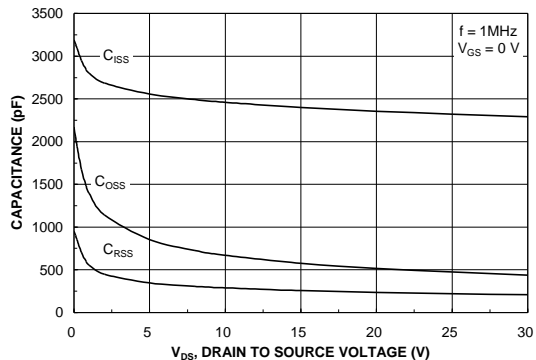

Figure 7. Gate Charge Characteristics

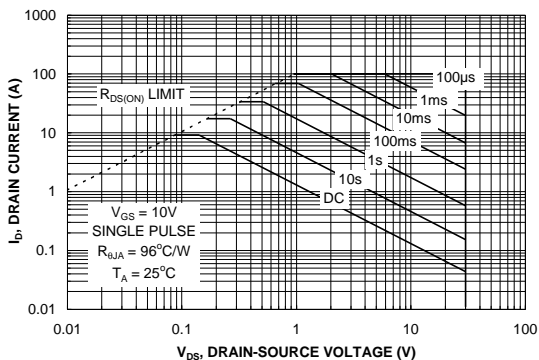**Figure 8. Capacitance Characteristics**

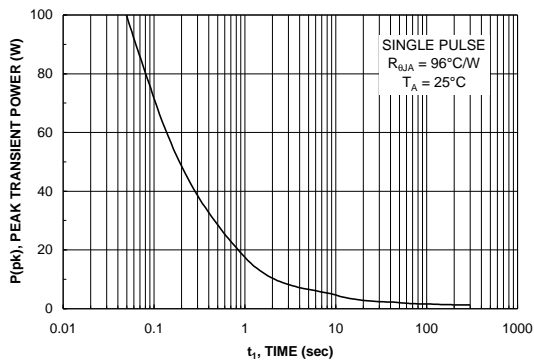
Figure 9. Maximum Safe Operating Area

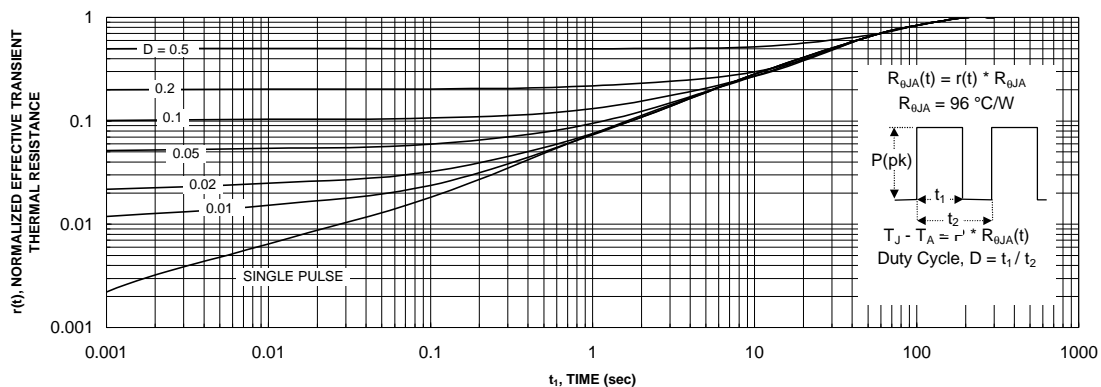**Figure 10. Single Pulse Maximum Power Dissipation**

Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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CoolFET™	FRFET™	MicroFET™	QFET®	SuperSOT™-8
CROSSVOLT™	GlobalOptoisolator™	MicroPak™	QS™	SyncFET™
DOME™	GTO™	MICROWIRE™	QT Optoelectronics™	TinyLogic®
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