

FDMS7650

N-Channel PowerTrench® MOSFET

30 V, 100 A, 0.99 mΩ

Features

- Max $r_{DS(on)}$ = 0.99 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 36\text{ A}$
- Max $r_{DS(on)}$ = 1.55 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 32\text{ A}$
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

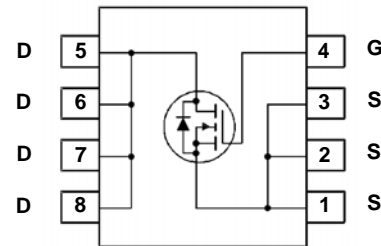
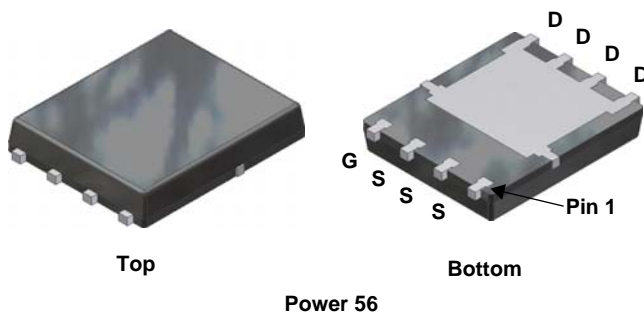


General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge and extremely low $r_{DS(on)}$.

Applications

- OringFET
- Synchronous rectifier



MOSFET Maximum Ratings $T_C = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 4)	±20	V
I_D	Drain Current -Continuous (Package limited) $T_C = 25\text{ °C}$	100	A
	-Continuous (Silicon limited) $T_C = 25\text{ °C}$	232	
	-Continuous $T_A = 25\text{ °C}$ (Note 1a)	36	
	-Pulsed	200	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	544	mJ
P_D	Power Dissipation $T_C = 25\text{ °C}$	104	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7650	FDMS7650	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		15		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 36\text{ A}$		0.8	0.99	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 32\text{ A}$		1.1	1.55	
		$V_{GS} = 10\text{ V}$, $I_D = 36\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		1.1	1.7	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 36\text{ A}$		267		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		11250	14965	pF
C_{oss}	Output Capacitance			3050	4055	pF
C_{riss}	Reverse Transfer Capacitance			240	360	pF
R_g	Gate Resistance			1.4	3	Ω

Switching Characteristics

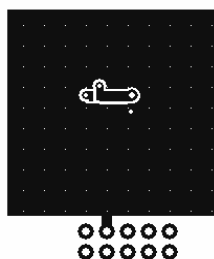
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 36\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		28	45	ns	
t_r	Rise Time			24	38	ns	
$t_{d(off)}$	Turn-Off Delay Time			83	133	ns	
t_f	Fall Time			21	34	ns	
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		149	209	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$	$V_{DD} = 15\text{ V}$, $I_D = 36\text{ A}$		63	88	nC
Q_{gs}	Gate to Source Charge				34		nC
Q_{gd}	Gate to Drain "Miller" Charge				13		nC

Drain-Source Diode Characteristics

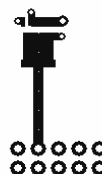
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2.1\text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = 36\text{ A}$ (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 36\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		69	97	ns
Q_{rr}	Reverse Recovery Charge			56	90	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b. 125 $^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 ms, Duty cycle < 2.0%.

3. Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1\text{ mH}$, $I_{AS} = 33\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 10\text{ V}$.

4. As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

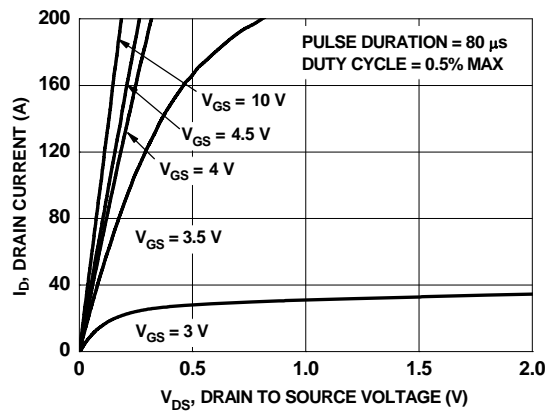


Figure 1. On Region Characteristics

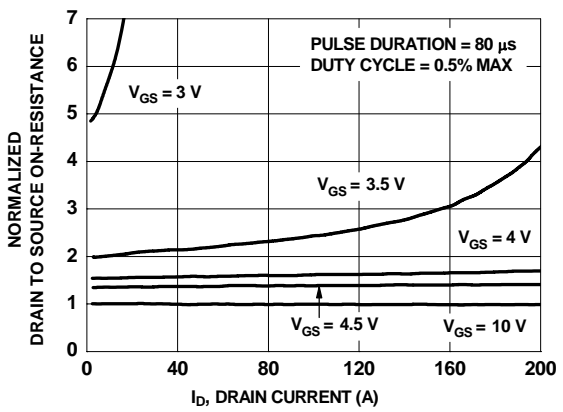


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

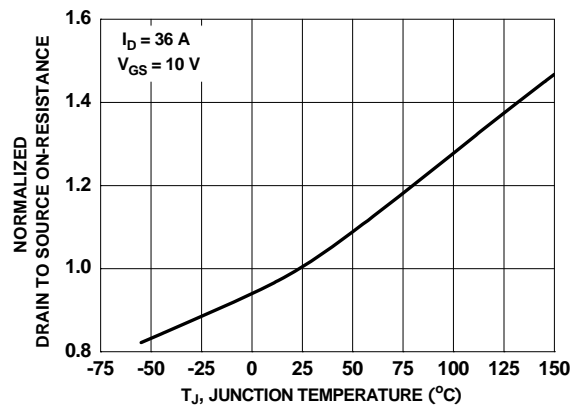


Figure 3. Normalized On Resistance vs Junction Temperature

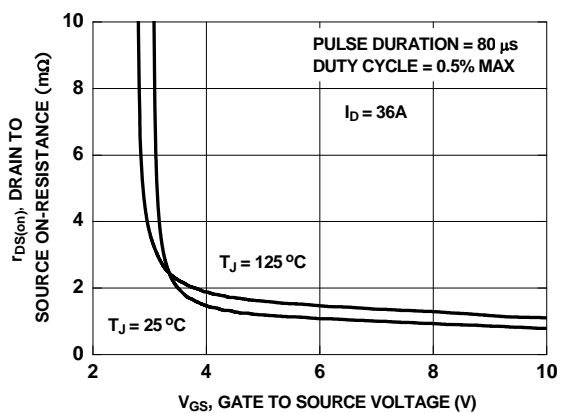


Figure 4. On-Resistance vs Gate to Source Voltage

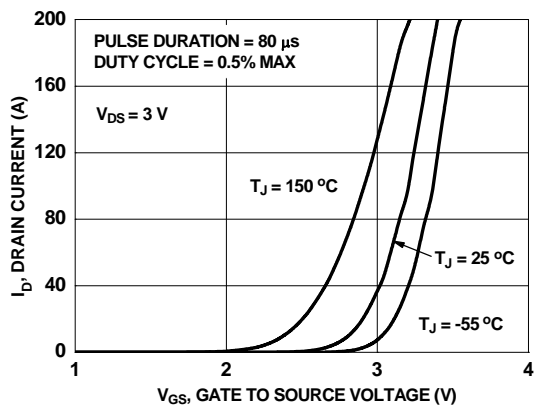


Figure 5. Transfer Characteristics

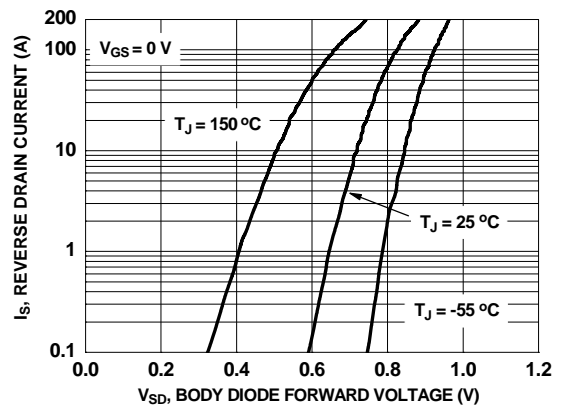


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

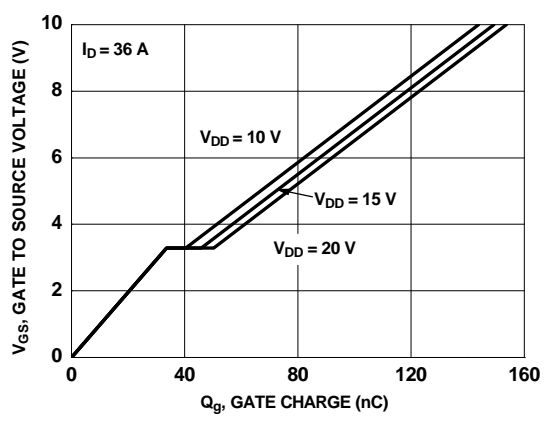


Figure 7. Gate Charge Characteristics

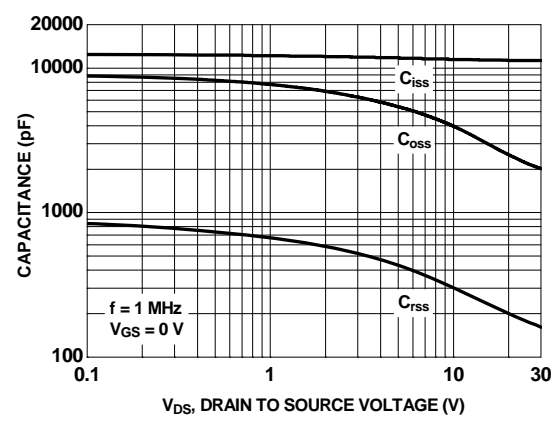


Figure 8. Capacitance vs Drain to Source Voltage

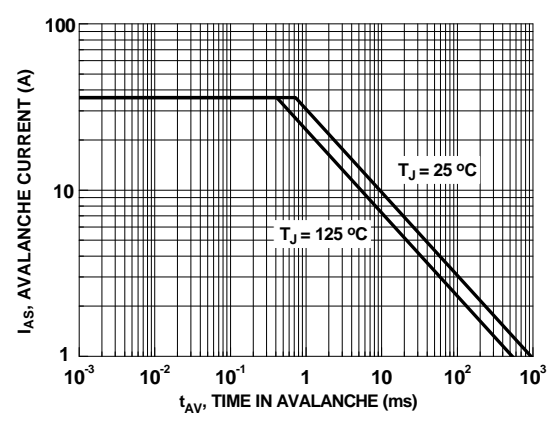


Figure 9. Unclamped Inductive Switching Capability

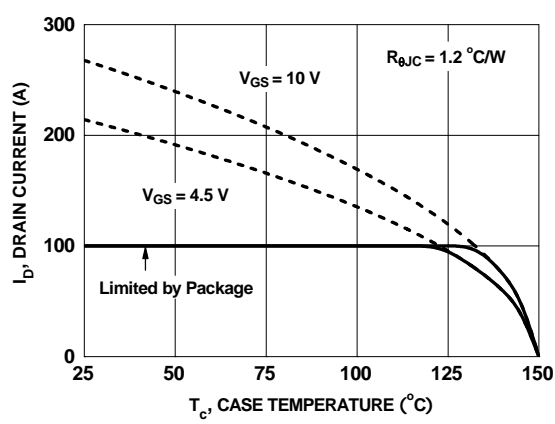


Figure 10. Maximum Continuous Drain Current vs Case Temperature

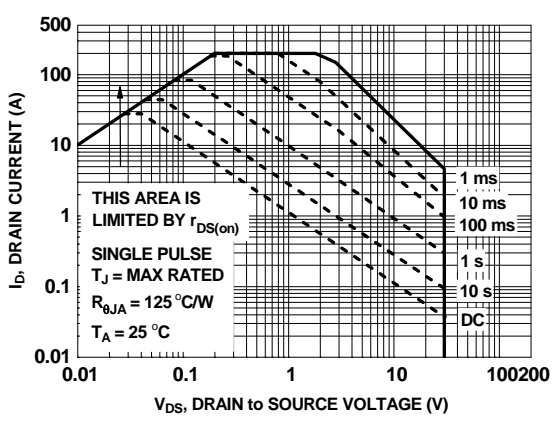


Figure 11. Forward Bias Safe Operating Area

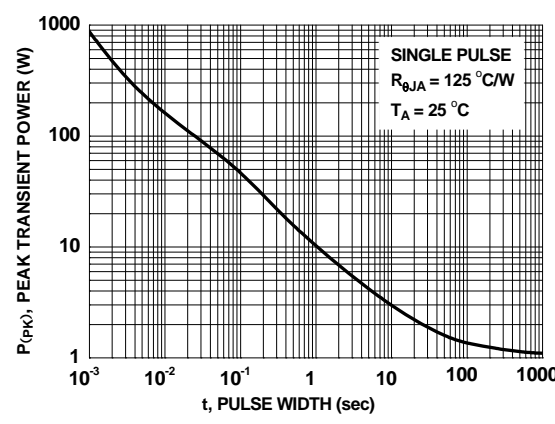


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

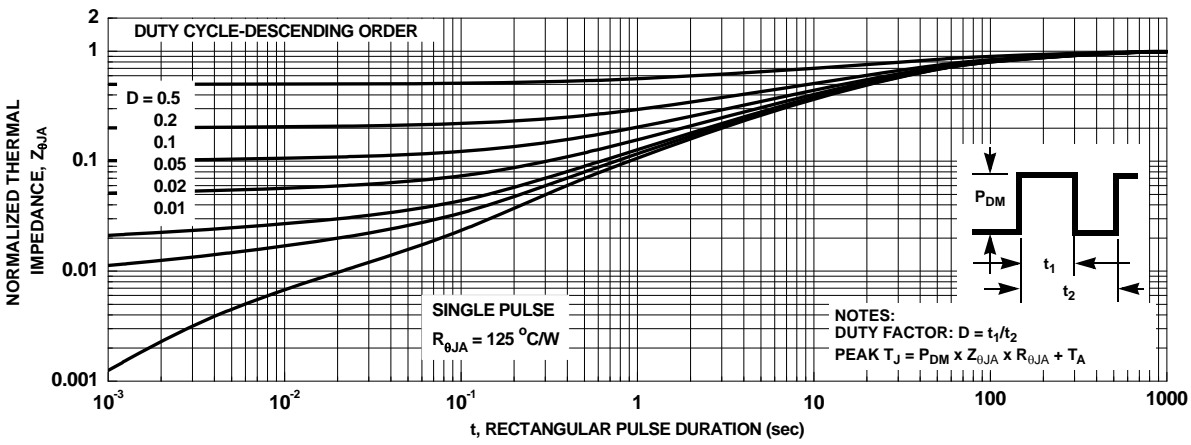
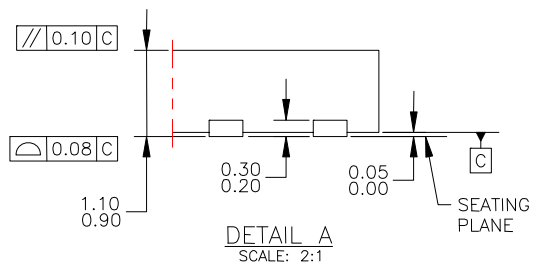
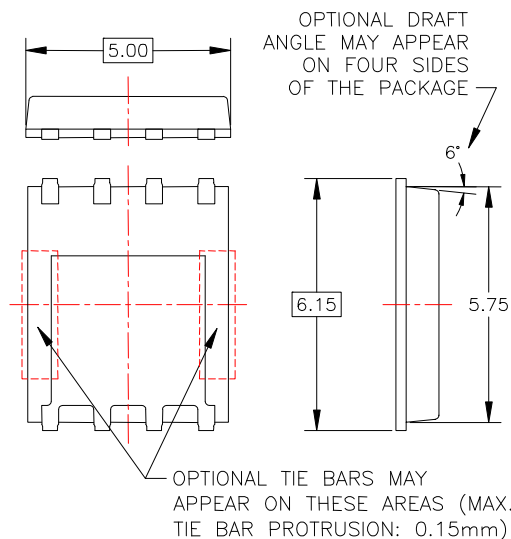
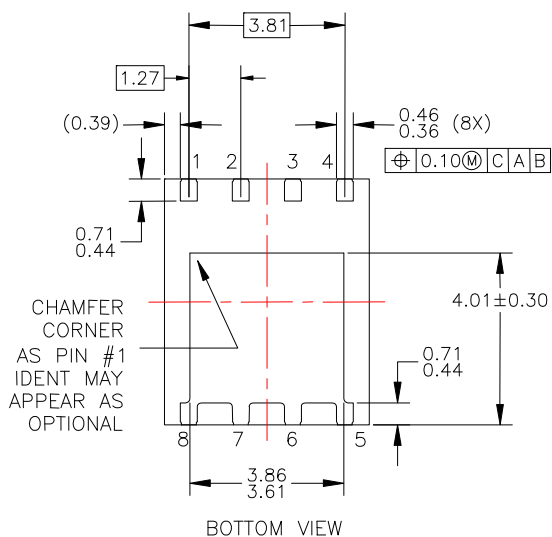
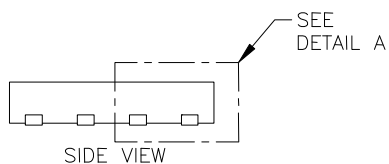
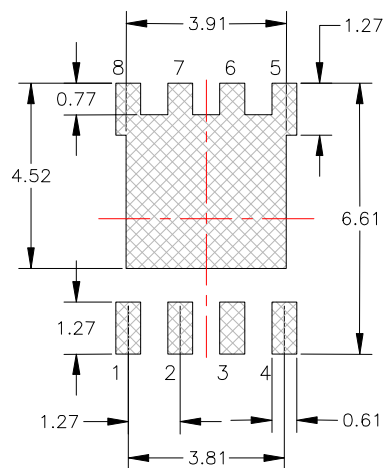
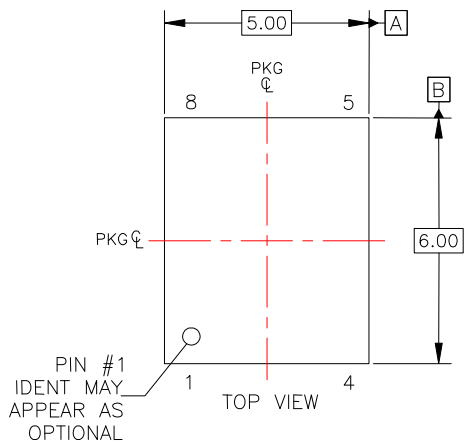


Figure 13. Junction-to-Ambient Transient Thermal Response Curve




Dimensional Outline and Pad Layout





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