

May 2012
UniFET TM

FDP5N50F / FDPF5N50FT N-Channel MOSFET, FRFET 500V, 4.5A, 1.55 Ω

Features

- $R_{DS(on)}$ = 1.25 Ω (Typ.)@ V_{GS} = 10V, I_D = 2.25A
- Low gate charge (Typ. 11nC)
- Low C_{rss} (Typ. 5pF)
- · Fast switching
- · 100% avalanche tested
- · Improved dv/dt capability
- · RoHS compliant



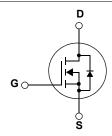
Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pluse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power suppliesand active power factor-correction.







MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol		Parameter			FDPF5N50FT	Units
V _{DSS}	Drain to Source Voltage	Drain to Source Voltage		500		V
V _{GSS}	Gate to Source Voltage			±	30	V
1	Drain Current	-Continuous (T _C = 25°C)		4.5	4.5*	۸
ID	Drain Current	-Continuous (T _C = 100°C)		2.7	2.7*	Α
I _{DM}	Drain Current	- Pulsed	(Note 1)	18	18*	Α
E _{AS}	Single Pulsed Avalanche Energy (Note 2)) 233		mJ	
I _{AR}	Avalanche Current		(Note 1)	4.5		Α
E _{AR}	Repetitive Avalanche Energy		(Note 1)	8.5		mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)) 4.5		V/ns
n	Dawer Dissipation	$(T_C = 25^{\circ}C)$		85	28	W
P_{D}	Power Dissipation	- Derate above 25°C		0.67	0.22	W/°C
T _J , T _{STG}	Operating and Storage Tempe	rature Range		-55 to	o +150	°C
T _L	Maximum Lead Temperature for 1/8" from Case for 5 Seconds	or Soldering Purpose,		3	00	°C
Drain current lir	mited by maximum junction temperati	ure	'		1	

Thermal Characteristics

Symbol	Parameter	FDP5N50F	FDPF5N50FT	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	4.5	
$R_{\theta CS}$	Thermal Resistance, Case to Sink Typ.	0.5	-	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	62.5	

Package Marking and Ordering Information T_C = 25°C unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP5N50F	FDP5N50F	TO-220	-	-	50
FDPF5N50FT	FDPF5N50FT	TO-220F	-	-	50

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Charac	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A$, $V_{GS} = 0 V$, $T_J = 25 ^{\circ} C$	500	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250μA, Referenced to 25°C	-	0.6	-	V/°C
I _{DSS} Zero Gate Voltage Drain Current	V _{DS} = 500V, V _{GS} = 0V	-	-	10		
	$V_{DS} = 400V, T_C = 125^{\circ}C$	-	-	100	μΑ	
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30V, V_{DS} = 0V$	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	3.0	-	5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10V, I_D = 2.25A$	ı	1.25	1.55	Ω
9 _{FS}	Forward Transconductance	$V_{DS} = 20V, I_D = 2.25A$ (Note 4)	ı	4.3	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	\\ - 25\\ \\ - 2\\	-	490	650	pF
C _{oss}	Output Capacitance	V _{DS} = 25V, V _{GS} = 0V f = 1MHz	-	66	88	pF
C _{rss}	Reverse Transfer Capacitance	T = TWITE	-	5	7.5	pF
Q _{g(tot)}	Total Gate Charge at 10V		-	11	15	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DS} = 400V, I_{D} = 5A$	-	3	-	nC
Q _{gd}	Gate to Drain "Miller" Charge	V _{GS} = 10V (Note 4, 5)	-	5	ı	nC

Switching Characteristics

t _{d(on)}	Turn-On Delay Time			-	13	36	ns
t _r	Turn-On Rise Time	$V_{DD} = 250V, I_D = 5A$		-	22	54	ns
t _{d(off)}	Turn-Off Delay Time	$R_G = 25\Omega$		-	28	66	ns
t _f	Turn-Off Fall Time		(Note 4, 5)	-	20	50	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	4.5	Α	
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	18	Α	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V, I_{SD} = 4.5A$		-	-	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _{SD} = 5A		-	65	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100A/\mu s$	(Note 4)	-	120	-	nC

- Notes: 1: Repetitive Rating: Pulse width limited by maximum junction temperature 2: L = 23 mH, I_{AS} = 4.5A, V_{DD} = 50V, R_{G} = 25 Ω , Starting T_{J} = 25 $^{\circ}$ C 3: I_{SD} ≤ 4.5A, di/dt ≤ 200A/ μ s, V_{DD} ≤ BV $_{DSS}$, Starting T_{J} = 25 $^{\circ}$ C 4: Pulse Test: Pulse width ≤ 300 μ s, Duty Cycle ≤ 2% 5: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

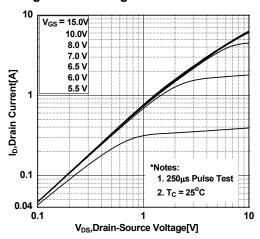


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

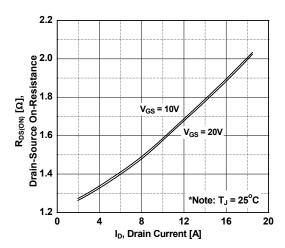


Figure 5. Capacitance Characteristics

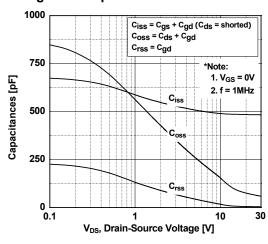


Figure 2. Transfer Characteristics

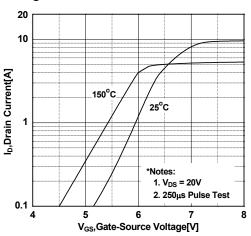


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

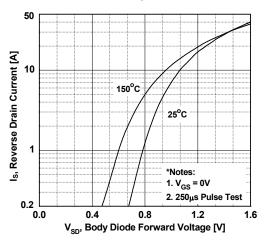
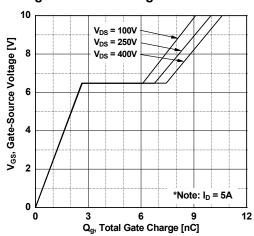
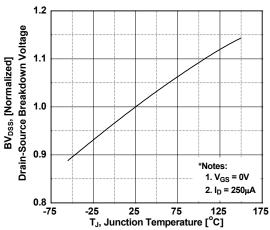


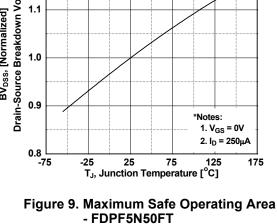
Figure 6. Gate Charge Characteristics

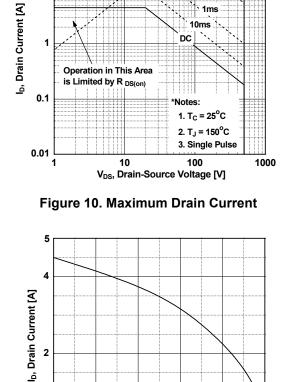


Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature







100

T_C, Case Temperature [°C]

150

Figure 8. Maximum Safe Operating Area

10ms DC

- FDP5N50F

Operation in This Area is Limited by R DS(on)

30

10

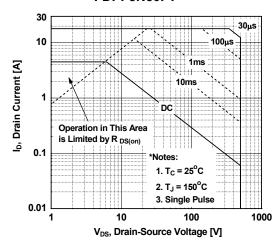
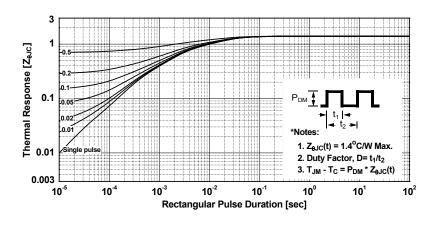


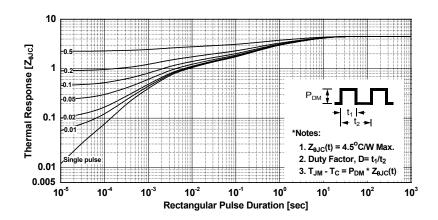
Figure 11. Transient Thermal Response Curve - FDP5N50F

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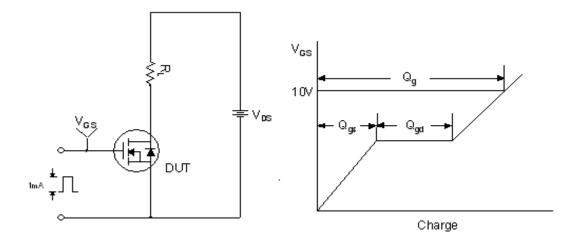


Typical Performance Characteristics (Continued)

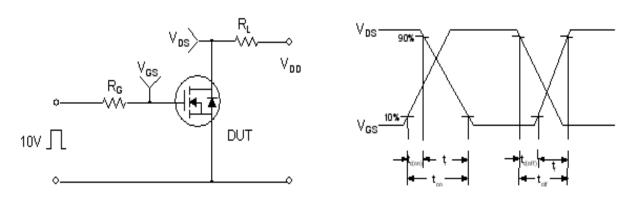




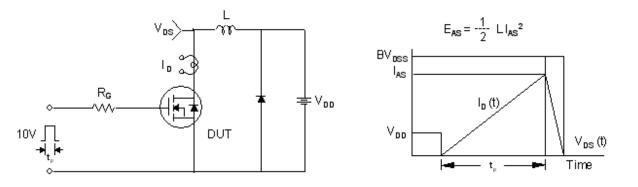
Gate Charge Test Circuit & Waveform



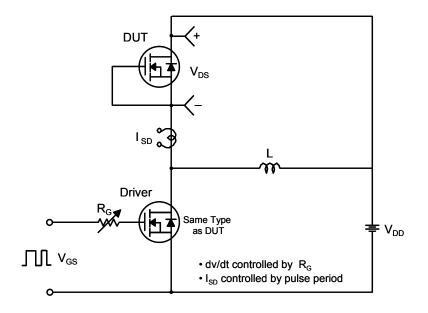
Resistive Switching Test Circuit & Waveforms

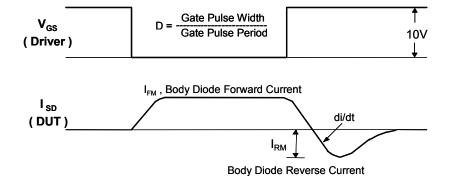


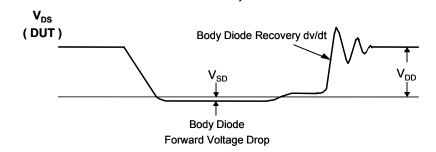
Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms

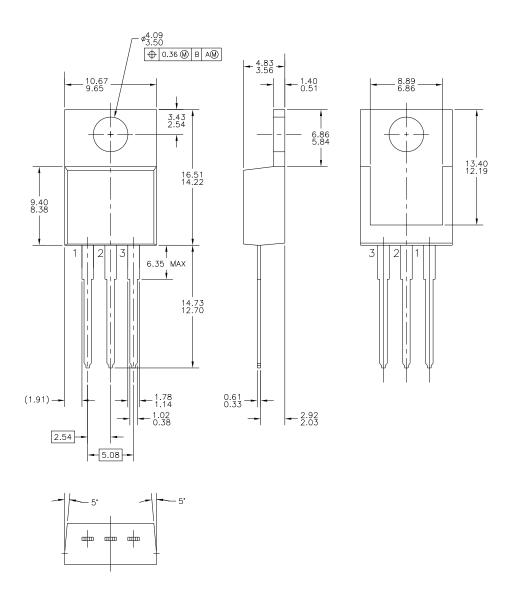






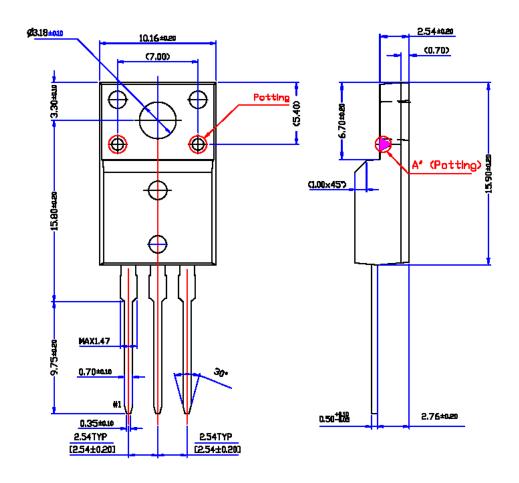
Mechanical Dimensions

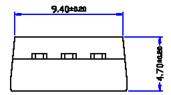
TO-220



Package Dimensions

TO-220F Potted





* Front/Back Side Isolation Voltage : AC 2500V

Dimensions in Millimeters





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