FAIRCHILD SEMICONDUCTOR®

June 2001

HGT1N30N60A4D

600V, SMPS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode

General Description

The HGT1N30N60A4D is a MOS gated high voltage switching device combining the best features of a MOSFETs and a bipolar transistor. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C. This IGBT is ideal for many high voltage switching applications operating at high frequencies where low conduction losses are essential. This device has been optimized for high frequency switch mode power supplies.

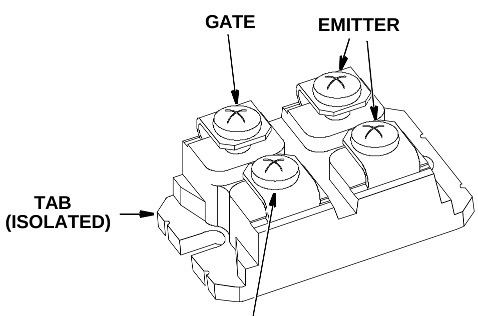
Formerly Developmental Type TA49345.

Features

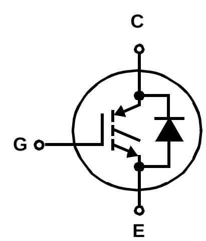
- 100kHz Operation At 390V, 20A
- 600V Switching SOA Capability
- Typical Fall Time . . . . 58ns at T_J = 125°C
- Low Conduction Loss

Package

JEDEC STYLE SOT-227



Symbol



Device Maximum Ratings T_C= 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
BV_{CES}	Collector to Emitter Breakdown Voltage	600	V
I_{C25}	Collector Current Continuous, At Starting T_C = 25°C	96	A
I_{C110}	Collector Current Continuous, At Starting T_C = 110°C	39	A
I_{CM}	Collector Current Pulsed (Note 1)	240	A
V_{GES}	Gate to Emitter Voltage Continuous	±20	V
V_{GEM}	Gate to Emitter Voltage Pulsed	±30	V
SSOA	Switching Safe Operating Area at T_J = 150°C, Figure 2	150A at 600V	
P_D	Power Dissipation Total T_C = 25°C	255	W
	Power Dissipation Derating T_C > 25°C	2.0	W/°C
V_{ISOL}	RMS Isolation Voltage, Any Terminal to Case, t = 1 min.	2500	V
T_J	Operating Junction Temperature Range	-55 to 150	°C
T_{STG}	Storage Junction Temperature Range	-55 to 150	°C
	Baseplate Screw Torque 4mm Metric Screw Size	1.5	N-m
	Terminal Screw Torque 4mm Metric Screw Size	1.7	N-m

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. Pulse width limited by maximum junction temperature.

Package Marking and Ordering Information

Device Marking	Device	Package	Tape Width	Quantity
30N60A4D	HGT1N30N60A4D	SOT-227	-	-

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Off State Characteristics							
BV_{CES}	Collector to Emitter Breakdown Voltage	I_C = 250μA, V_{GE} = 0		600	-	-	V
I_{CES}	Collector to Emitter Leakage Current	V_{CE} = 600V	T_J = 25°C	-	-	250	μA
			T_J = 125°C	-	-	2.8	mA
I_{GES}	Gate to Emitter Leakage Current	V_{GE} = ± 20V		-	-	±250	nA
On State Characteristics							
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_C = 30A, V_{GE} = 15V	T_J = 25°C	-	1.8	2.7	V
			T_J = 125°C	-	1.6	2.0	V
V_{EC}	Diode Forward Voltage	I_{EC} = 30A		-	2.2	2.5	V
Dynamic Characteristics							
$Q_{G(ON)}$	Gate Charge	I_C = 30A, V_{CE} = 300V	V_{GE} = 15V	-	225	270	nC
			V_{GE} = 20V	-	300	360	nC
$V_{GE(TH)}$	Gate to Emitter Threshold Voltage	I_C = 250μA, V_{CE} = 600V		4.5	5.2	7.0	V
V_{GEP}	Gate to Emitter Plateau Voltage	I_C = 30A, V_{CE} = 300V		-	8.5	-	V
Switching Characteristics							
SSOA	Switching SOA	T_J = 150°C, R_G = 3Ω, V_{GE} = 15V, L = 100μH, V_{CE} = 600V		150	-	-	A
$t_{d(ON)I}$	Current Turn-On Delay Time	IGBT and Diode at T_J = 25°C, I_{CE} = 30A, V_{CE} = 390V, V_{GE} = 15V, R_G = 3Ω L = 200μH Test Circuit - Figure 24		-	25	-	ns
t_{rI}	Current Rise Time			-	12	-	ns
$t_{d(OFF)I}$	Current Turn-Off Delay Time			-	150	-	ns
t_{fI}	Current Fall Time			-	38	-	ns
E_{ON1}	Turn-On Energy (Note 2)			-	280	-	μJ
E_{ON2}	Turn-On Energy (Note 2)			-	600	-	μJ
E_{OFF}	Turn-Off Energy (Note 3)			-	240	350	μJ
$t_{d(ON)I}$	Current Turn-On Delay Time	IGBT and Diode at T_J = 125°C I_{CE} = 30A, V_{CE} = 390V, V_{GE} = 15V, R_G = 3Ω L = 200μH Test Circuit - Figure 24		-	24	-	ns
t_{rI}	Current Rise Time			-	11	-	ns
$t_{d(OFF)I}$	Current Turn-Off Delay Time			-	180	200	ns
t_{fI}	Current Fall Time			-	58	70	ns
E_{ON1}	Turn-On Energy (Note 2)			-	280	-	μJ
E_{ON2}	Turn-On Energy (Note 2)			-	1000	1200	μJ
E_{OFF}	Turn-Off Energy (Note 3)			-	450	750	μJ
t_{rr}	Diode Reverse Recovery Time	I_{EC} = 30A, dI_{EC}/dt = 200A/μs		-	40	55	ns
		I_{EC} = 1A, dI_{EC}/dt = 200A/μs		-	30	42	ns
Thermal Characteristics							
$R_{\theta JC}$	Thermal Resistance Junction-Case	IGBT		-	-	0.49	°C/W
		Diode				2.0	°C/W

NOTE:

2. Values for two Turn-On loss conditions are shown for the convenience of the circuit designer. E_{ON1} is the turn-on loss of the IGBT only. E_{ON2} is the turn-on loss when a typical diode is used in the test circuit and the diode is at the same T_J as the IGBT. The diode type is specified in figure 24.

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A). All devices were tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

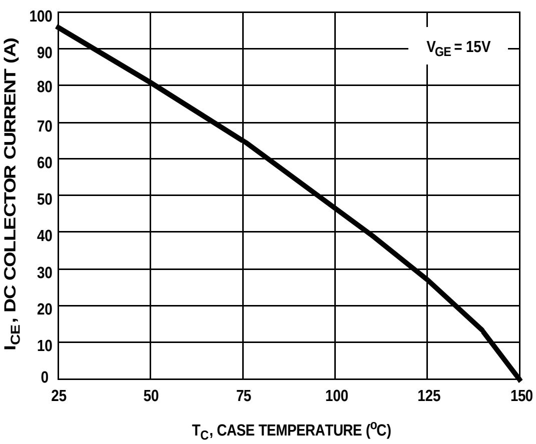


Figure 1. DC Collector Current vs Case Temperature

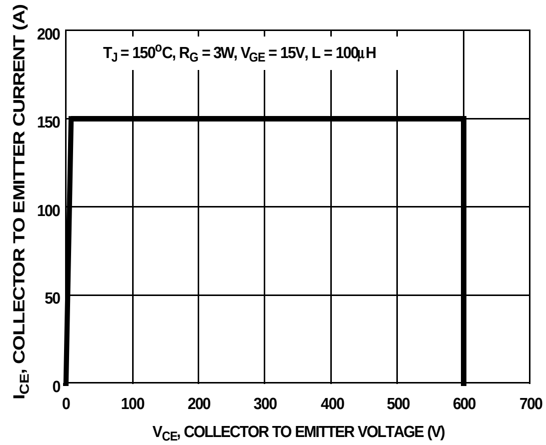


Figure 2. Minimum Switching Safe Operating Area

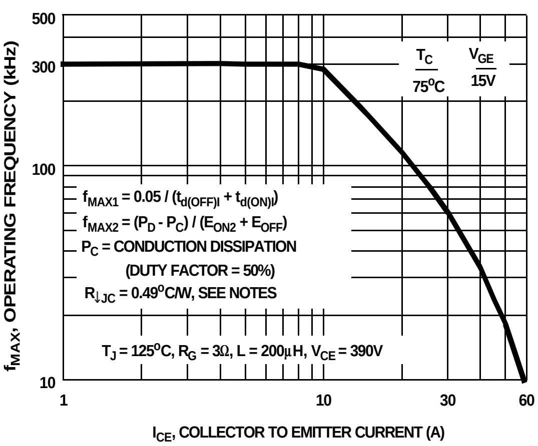


Figure 3. Operating Frequency vs Collector to Emitter Current

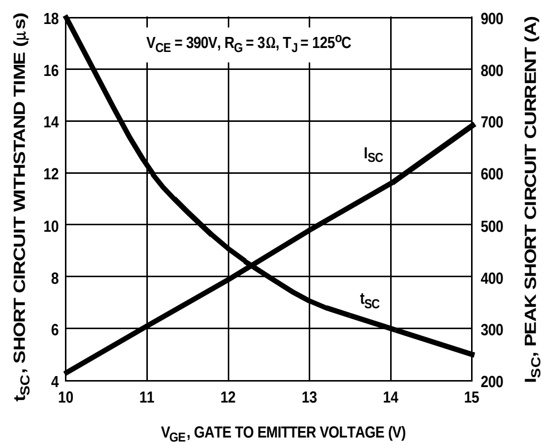


Figure 4. Short Circuit Withstand Time

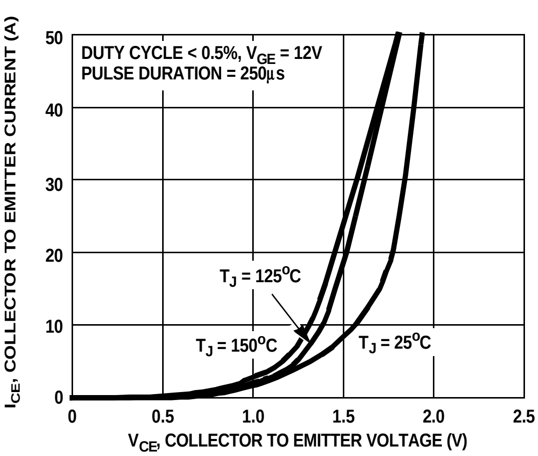


Figure 5. Collector to Emitter On-State Voltage

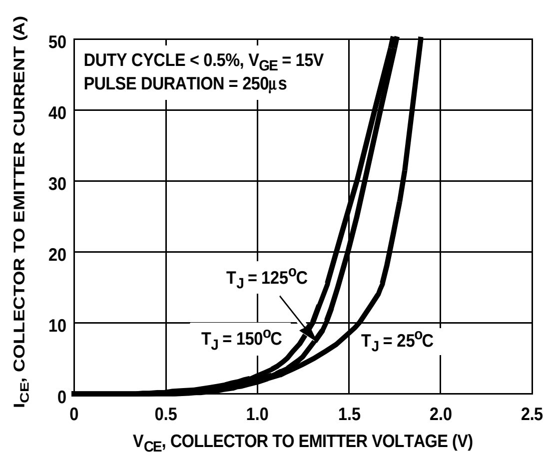


Figure 6. Collector to Emitter On-State Voltage

Typical Performance Curves (Continued)

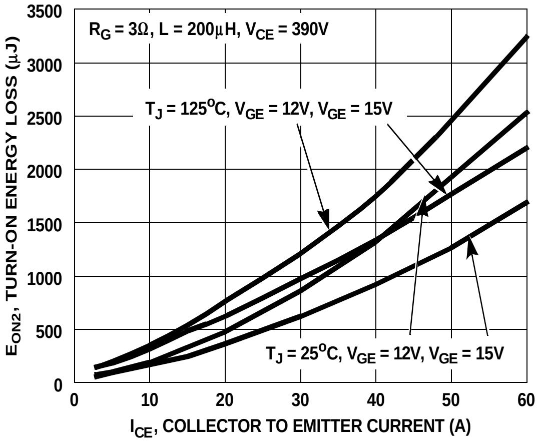


Figure 7. Turn-On Energy Loss vs Collector to Emitter Current

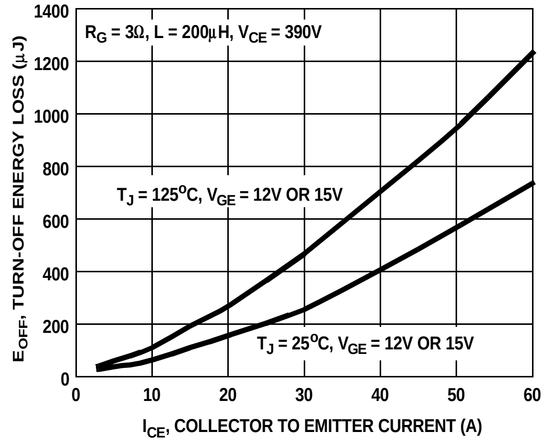


Figure 8. Turn-Off Energy Loss vs Collector to Emitter Current

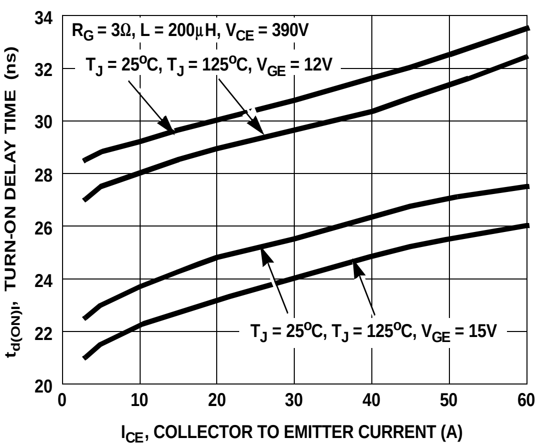


Figure 9. Turn-On Delay Time vs Collector to Emitter Current

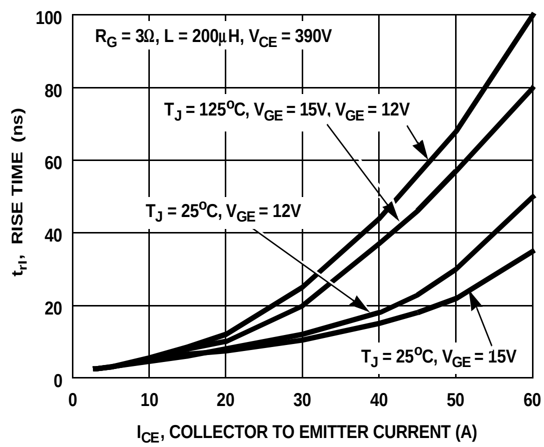


Figure 10. Turn-On Rise Time vs Collector to Emitter Current

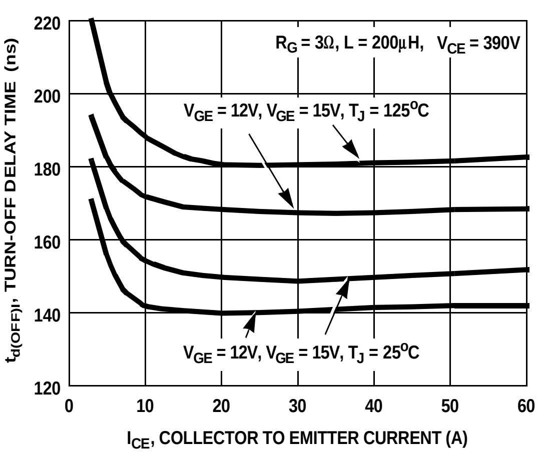


Figure 11. Turn-Off Delay Time vs Collector to Emitter Current

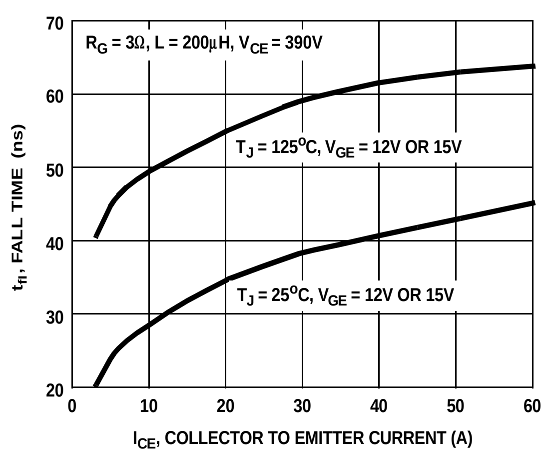


Figure 12. Fall Time vs Collector to Emitter Current

Typical Performance Curves (Continued)

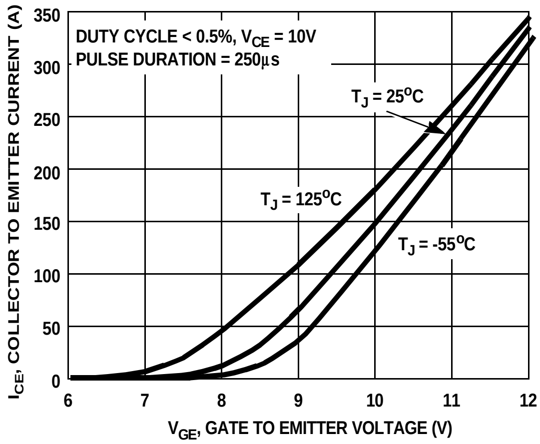


Figure 13. Transfer Characteristic

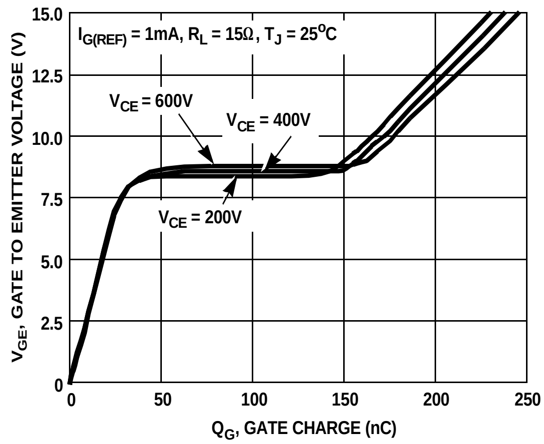


Figure 14. Gate Charge

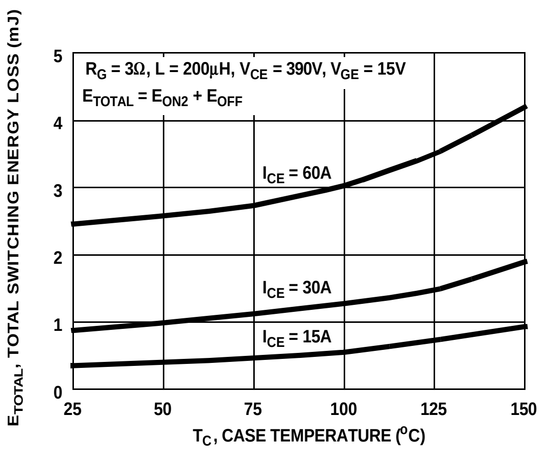


Figure 15. Total Switching Loss vs Case Temperature

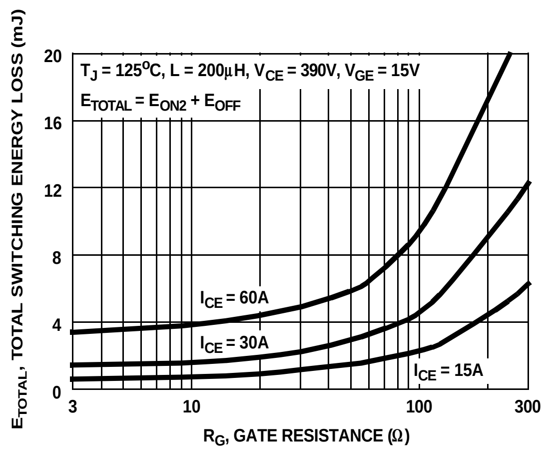


Figure 16. Total Switching Loss vs Gate Resistance

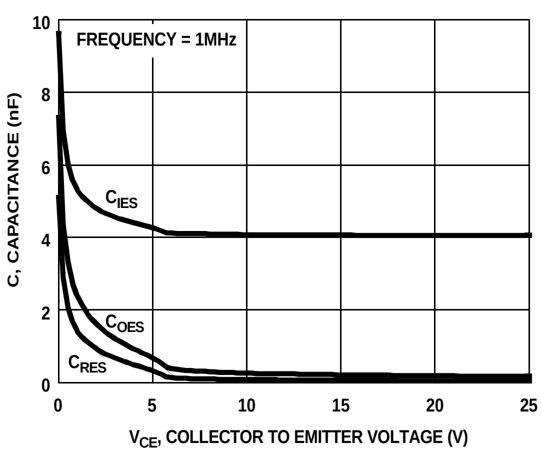


Figure 17. Capacitance vs Collector to Emitter Voltage

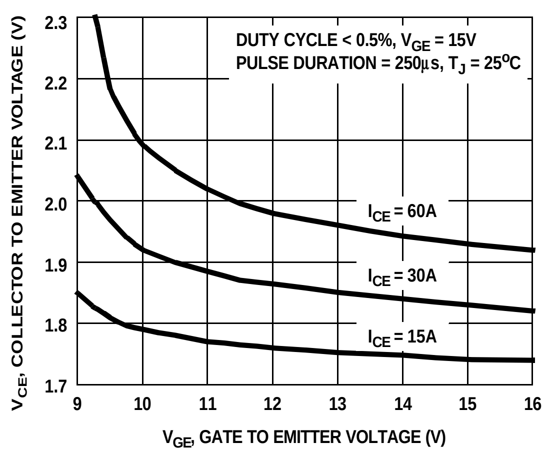


Figure 18. Collector to Emitter On-State Voltage vs Gate to Emitter Voltage

Typical Performance Curves (Continued)

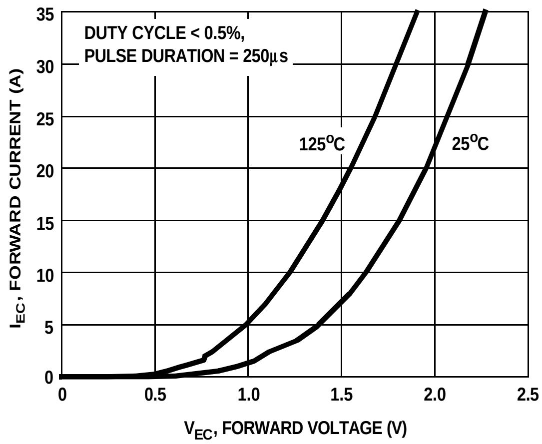


Figure 19. Diode Forward Current vs Forward Voltage Drop

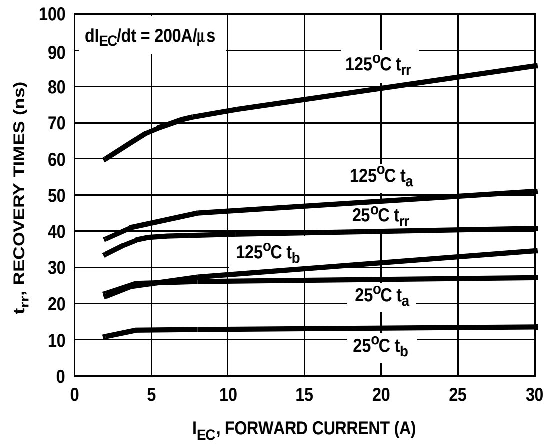


Figure 20. Recovery Times vs Forward Current

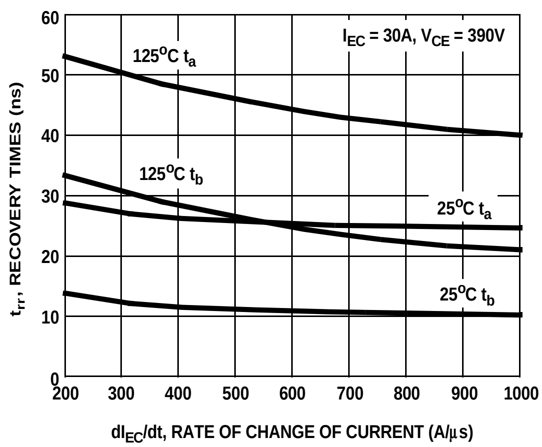


Figure 21. Recovery Times vs Rate of Change of Current

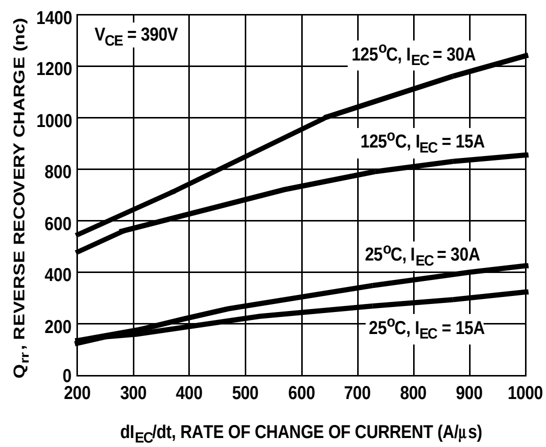


Figure 22. Stored Charge vs Rate of Change of Current

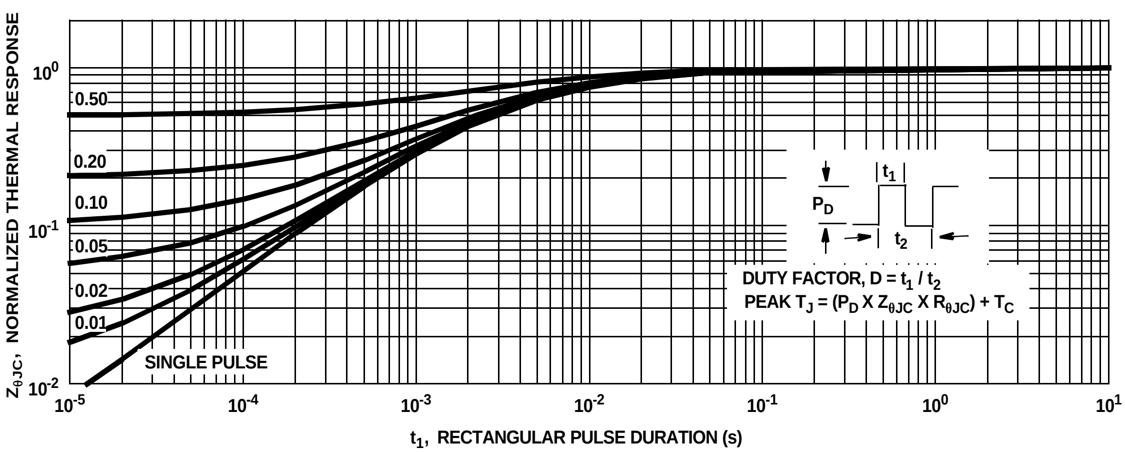


Figure 23. IGBT Normalized Transient Thermal Impedance, Junction to Case

Test Circuit and Waveforms

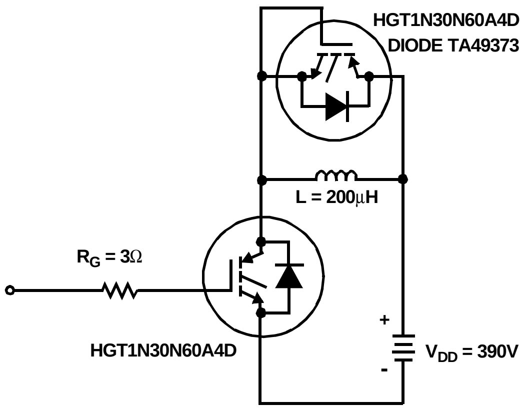


Figure 24. Inductive Switching Test Circuit

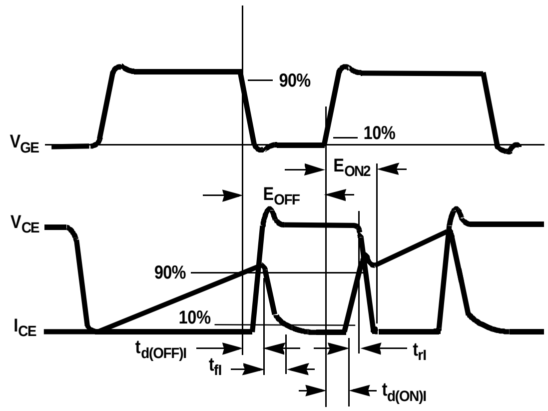


Figure 25. Switching Test Waveforms

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as “ECCOSORBD™ LD26” or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

Operating Frequency Information

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 5, 6, 7, 8, 9 and 11. The operating frequency plot (Figure 3) of a typical device shows f_{MAX1} or f_{MAX2}; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{d(OFF)I} + t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 25. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JM}. $t_{d(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON2})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JM} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 3) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON2} and E_{OFF} are defined in the switching waveforms shown in Figure 25. E_{ON2} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e., the collector current equals zero ($I_{CE} = 0$)

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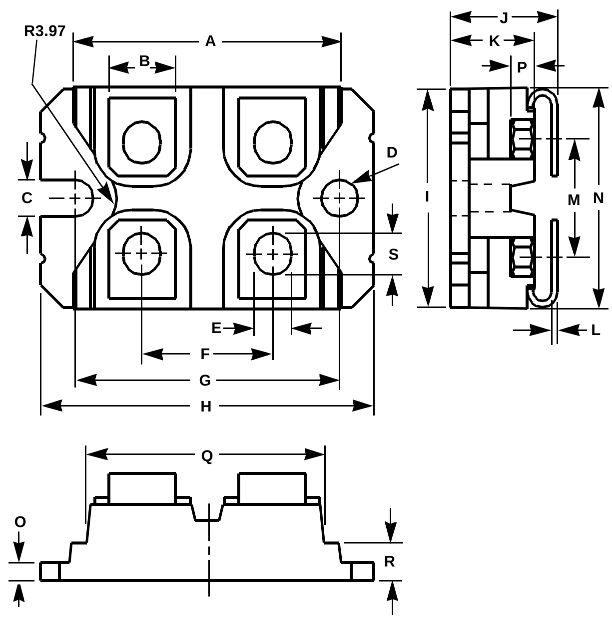
ISOTOP PACKAGE



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	1.240	1.255	31.50	31.88	-
B	0.310	0.322	7.87	8.18	-
C	0.163	0.169	4.14	4.29	-
D	0.163	0.169	4.14	4.29	-
E	0.165	0.169	4.19	4.29	-
F	0.588	0.594	14.99	15.09	-
G	1.186	1.192	30.12	30.28	-
H	1.494	1.504	37.95	38.20	-
I	0.976	0.986	24.79	25.04	-
J	0.472	0.480	11.99	12.19	-
K	0.372	0.378	9.45	9.60	-
L	0.030	0.033	0.76	0.84	-
M	0.495	0.506	12.57	12.85	-
N	0.990	1.000	25.15	25.40	-
O	0.080	0.084	2.03	2.13	-
P	0.108	0.124	2.74	3.15	-
Q	1.049	1.059	26.64	26.90	-
R	0.164	0.174	4.16	4.42	-
S	0.186	0.191	4.72	4.85	-

Rev. 0 8/00

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.