

June 1996

14A, 600V, UFS Series N-Channel IGBT

### Features

- 14A, 600V at  $T_C = +25^\circ\text{C}$
- 600V Switching SOA Capability
- Typical Fall Time - 140ns at  $T_J = +150^\circ\text{C}$
- Short Circuit Rating
- Low Conduction Loss

### Description

The HGTD7N60C3, HGTD7N60C3S and HGTP7N60C3 are MOS gated high voltage switching devices combining the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between  $+25^\circ\text{C}$  and  $+150^\circ\text{C}$ .

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

#### PACKAGING AVAILABILITY

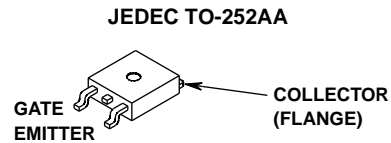
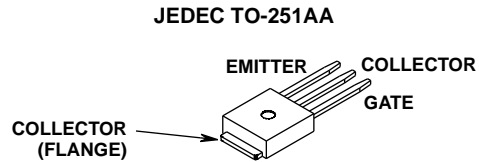
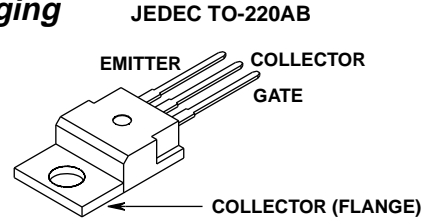
PART NUMBER	PACKAGE	BRAND
HGTD7N60C3	TO-251AA	G7N60C
HGTD7N60C3S	TO-252AA	G7N60C
HGTP7N60C3	TO-220AB	G7N60C3

NOTE: When ordering, use the entire part number.

Add the suffix 9A to obtain the TO-252AA variant in tape and reel, i.e. HGTD7N60C3S9A.

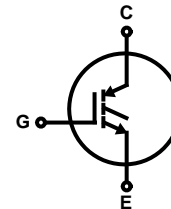
Formerly Developmental Type TA49115.

### Packaging



### Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



### Absolute Maximum Ratings $T_C = +25^\circ\text{C}$ , Unless Otherwise Specified

	HGTD7N60C3, HGTD7N60C3S HGTP7N60C3	UNITS
Collector-Emitter Voltage	600	V
Collector Current Continuous		
At $T_C = +25^\circ\text{C}$	14	A
At $T_C = +110^\circ\text{C}$	7	A
Collector Current Pulsed (Note 1)	56	A
Gate-Emitter Voltage Continuous	$\pm 20$	V
Gate-Emitter Voltage Pulsed	$\pm 30$	V
Switching Safe Operating Area at $T_J = +150^\circ\text{C}$ , Figure 14	40A at 480V	
Power Dissipation Total at $T_C = +25^\circ\text{C}$	60	W
Power Dissipation Derating $T_C > +25^\circ\text{C}$	0.48	W/ $^\circ\text{C}$
Reverse Voltage Avalanche Energy	100	mJ
Operating and Storage Junction Temperature Range	-40 to +150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering	260	$^\circ\text{C}$
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15\text{V}$	1	$\mu\text{s}$
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10\text{V}$	8	$\mu\text{s}$

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2.  $V_{CE(PK)} = 360\text{V}$ ,  $T_J = +125^\circ\text{C}$ ,  $R_{GE} = 50\Omega$ .

## Specifications HGTD7N60C3, HGTD7N60C3S, HGTP7N60C3

### Electrical Specifications $T_C = +25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Collector-Emitter Breakdown Voltage	$BV_{CES}$	$I_C = 250\mu\text{A}$ , $V_{GE} = 0\text{V}$	600	-	-	V	
Emitter-Collector Breakdown Voltage	$BV_{ECS}$	$I_C = 3\text{mA}$ , $V_{GE} = 0\text{V}$	16	30	-	V	
Collector-Emitter Leakage Current	$I_{CES}$	$V_{CE} = BV_{CES}$ , $T_C = +25^\circ\text{C}$	-	-	250	$\mu\text{A}$	
		$V_{CE} = BV_{CES}$ , $T_C = +150^\circ\text{C}$	-	-	2.0	$\text{mA}$	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$ , $V_{GE} = 15\text{V}$ , $T_C = +25^\circ\text{C}$	-	1.6	2.0	V	
		$T_C = +150^\circ\text{C}$	-	1.9	2.4	V	
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu\text{A}$ , $V_{CE} = V_{GE}$ , $T_C = +25^\circ\text{C}$	3.0	5.0	6.0	V	
Gate-Emitter Leakage Current	$I_{GES}$	$V_{GE} = \pm 25\text{V}$	-	-	$\pm 250$	$\text{nA}$	
Switching SOA	SSOA	$T_J = +150^\circ\text{C}$ $R_G = 50\Omega$ $V_{GE} = 15\text{V}$ $L = 1\text{mH}$	$V_{CE(PK)} = 480\text{V}$	40	-	-	A
			$V_{CE(PK)} = 600\text{V}$	6	-	-	A
Gate-Emitter Plateau Voltage	$V_{GEP}$	$I_C = I_{C110}$ , $V_{CE} = 0.5 BV_{CES}$	-	8	-	V	
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$ , $V_{CE} = 0.5 BV_{CES}$	$V_{GE} = 15\text{V}$	-	23	30	$\text{nC}$
			$V_{GE} = 20\text{V}$	-	30	38	$\text{nC}$
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = 150^\circ\text{C}$ $I_{CE} = I_{C110}$ $V_{CE(PK)} = 0.8 BV_{CES}$ $V_{GE} = 15\text{V}$ $R_G = 50\Omega$ $L = 1.0\text{mH}$	-	8.5	-	$\text{ns}$	
Current Rise Time	$t_{RI}$		-	11.5	-	$\text{ns}$	
Current Turn-Off Delay Time	$t_{D(OFF)I}$		-	350	400	$\text{ns}$	
Current Fall Time	$t_{FI}$		-	140	275	$\text{ns}$	
Turn-On Energy	$E_{ON}$		-	165	-	$\mu\text{J}$	
Turn-Off Energy (Note 1)	$E_{OFF}$		-	600	-	$\mu\text{J}$	
Thermal Resistance	$R_{\theta JC}$		-	-	2.1	$^\circ\text{C/W}$	

**NOTE:**

- Turn-Off Energy Loss ( $E_{OFF}$ ) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ( $I_{CE} = 0\text{A}$ ). The HGTD7N60C3, HGTD7N60C3S and HGTP7N60C3 were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include diode losses.

**HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:**

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951

Typical Performance Curves

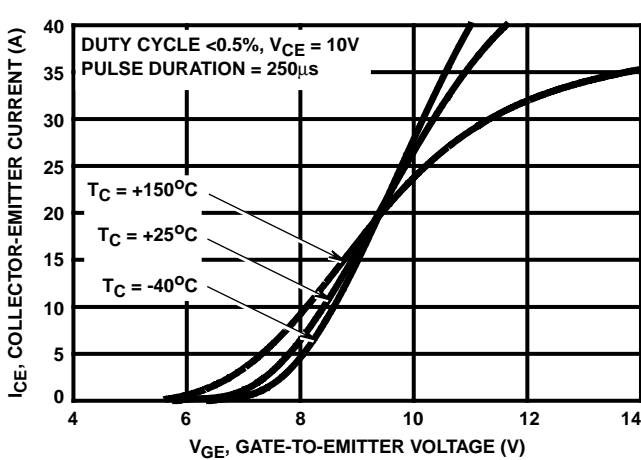


FIGURE 1. TRANSFER CHARACTERISTICS

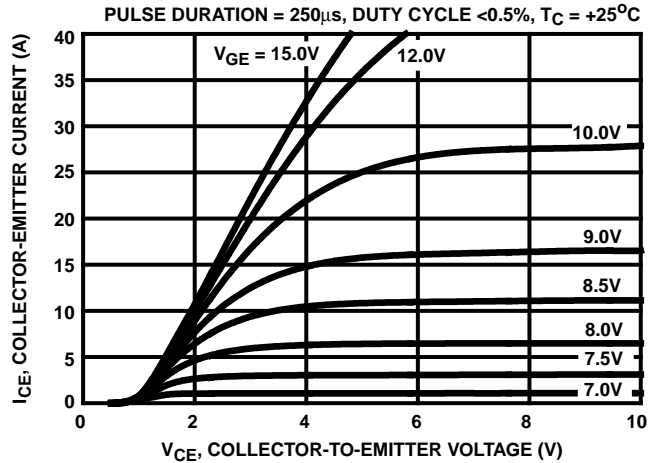


FIGURE 2. SATURATION CHARACTERISTICS

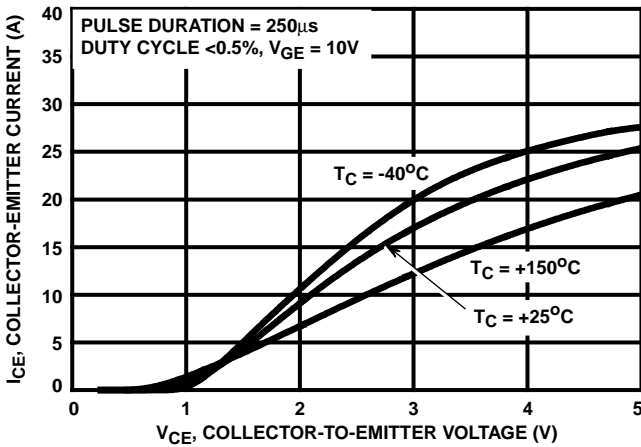


FIGURE 3. COLLECTOR-EMITTER ON - STATE VOLTAGE

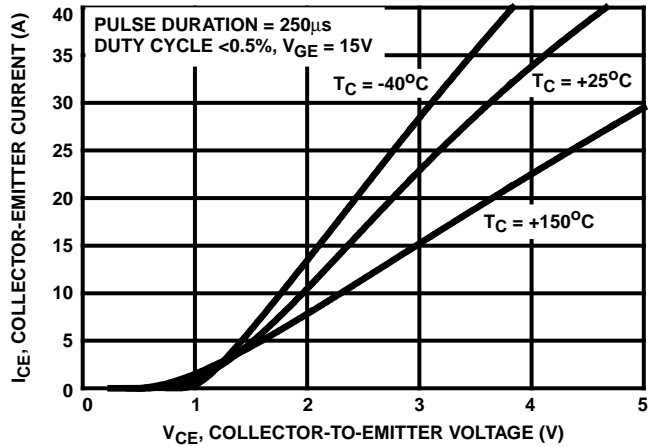


FIGURE 4. COLLECTOR-EMITTER ON - STATE VOLTAGE

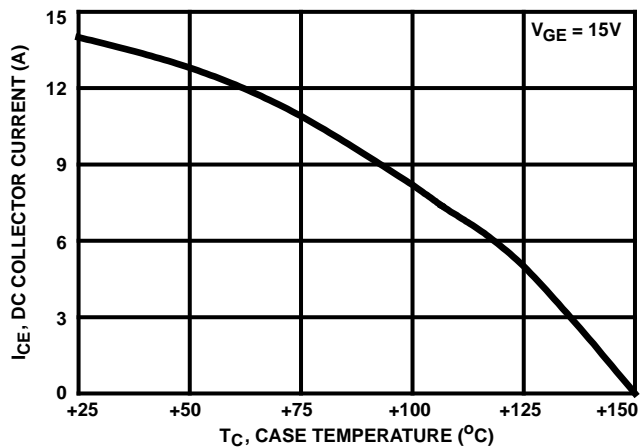


FIGURE 5. MAXIMUM DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

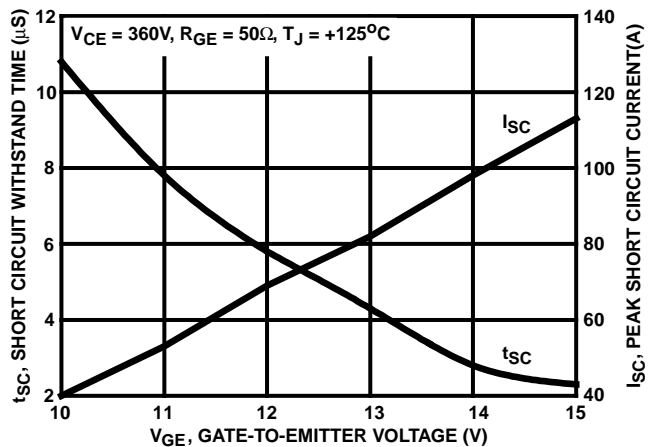


FIGURE 6. SHORT CIRCUIT WITHSTAND TIME

Typical Performance Curves (Continued)

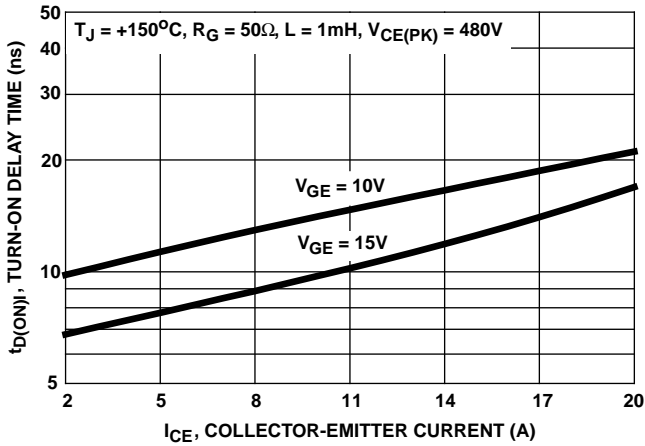


FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

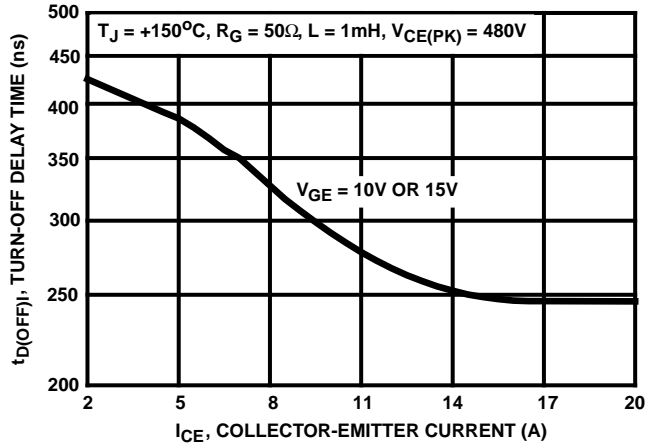


FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

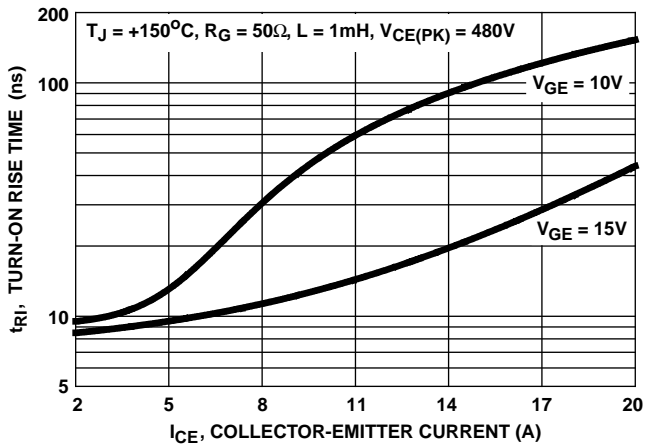


FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

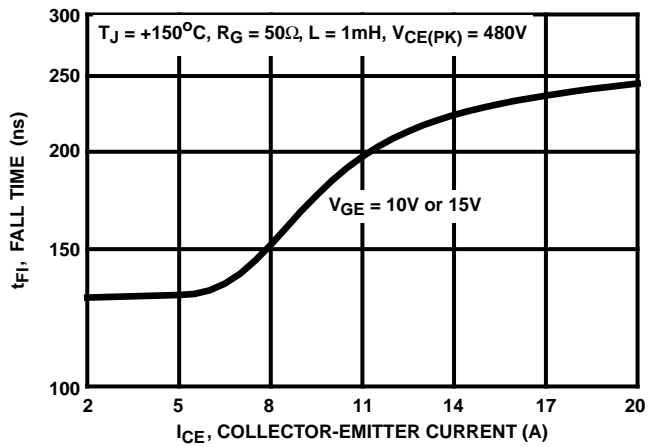


FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

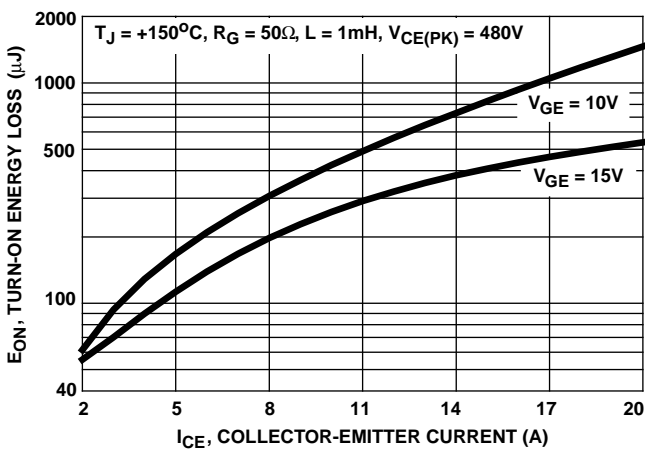


FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

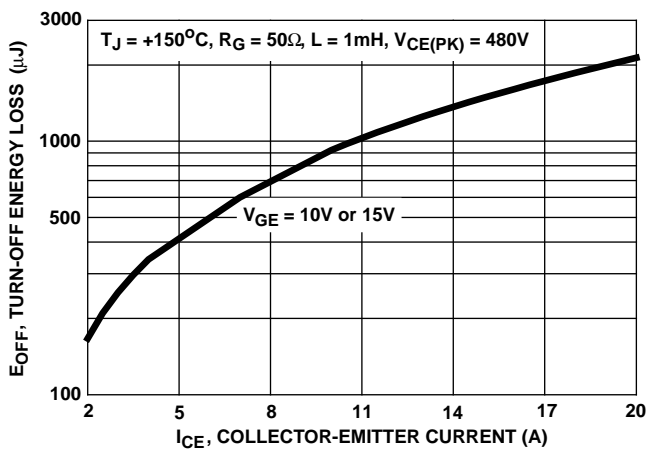


FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

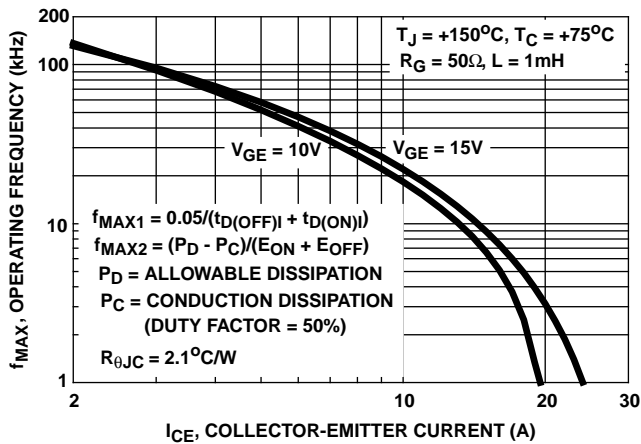


FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

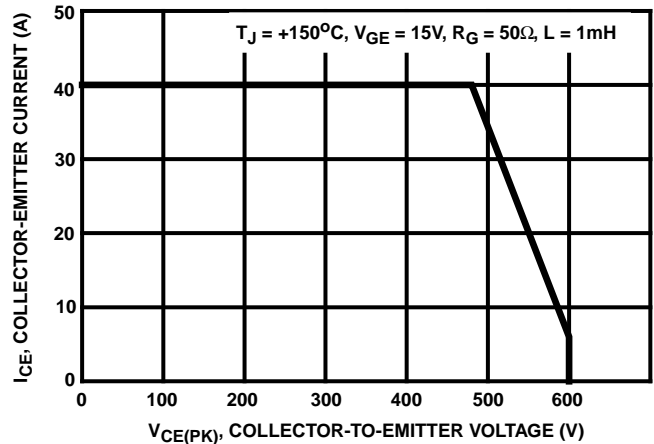


FIGURE 14. MINIMUM SWITCHING SAFE OPERATING AREA

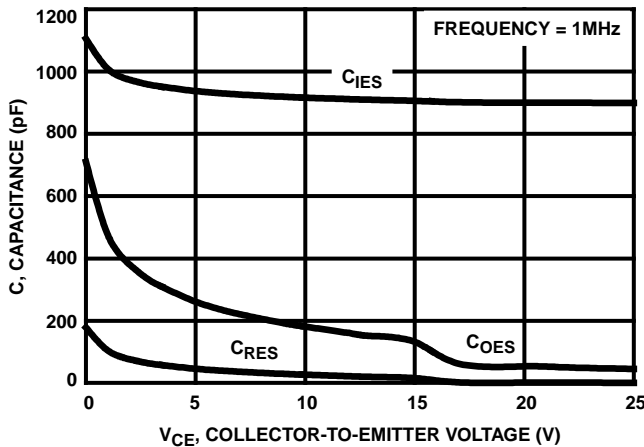


FIGURE 15. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

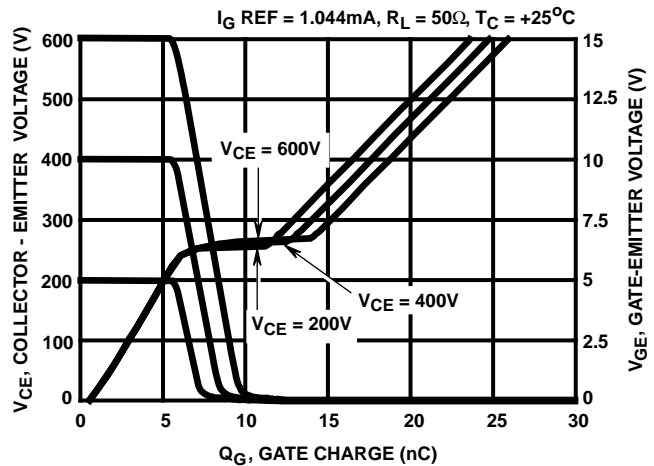


FIGURE 16. GATE CHARGE WAVEFORMS

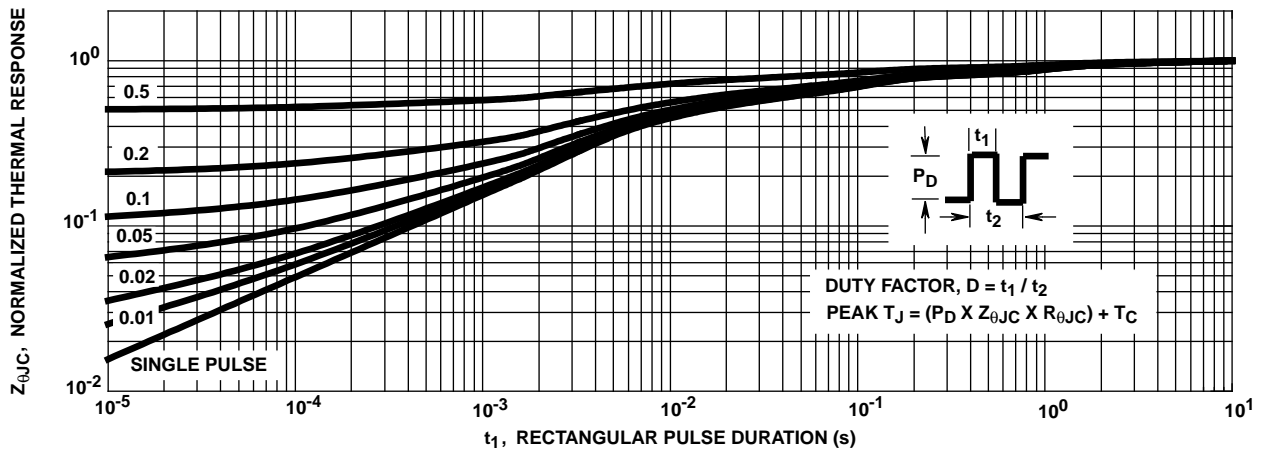


FIGURE 17. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

### Test Circuit and Waveforms

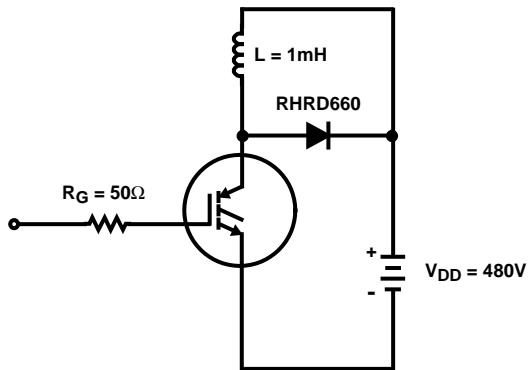


FIGURE 18. INDUCTIVE SWITCHING TEST CIRCUIT

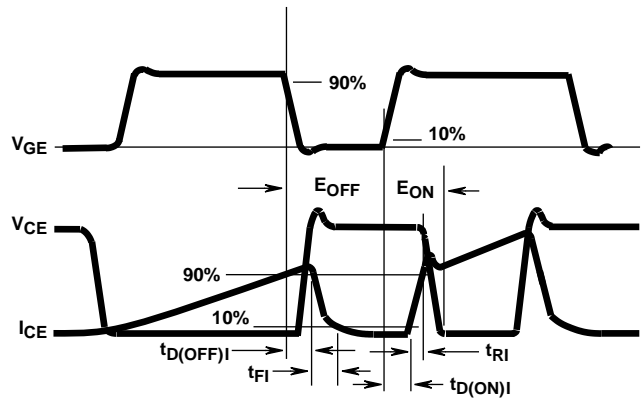


FIGURE 19. SWITCHING TEST WAVEFORMS

### Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as †"ECCOSORB LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of  $V_{GEM}$ . Exceeding the rated  $V_{GE}$  can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

† Trademark Emerson and Cumming, Inc.

### Operating Frequency Information

#### Operating Frequency Information for a Typical Device

Figure 13 is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current ( $I_{CE}$ ) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows  $f_{MAX1}$  or  $f_{MAX2}$  whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

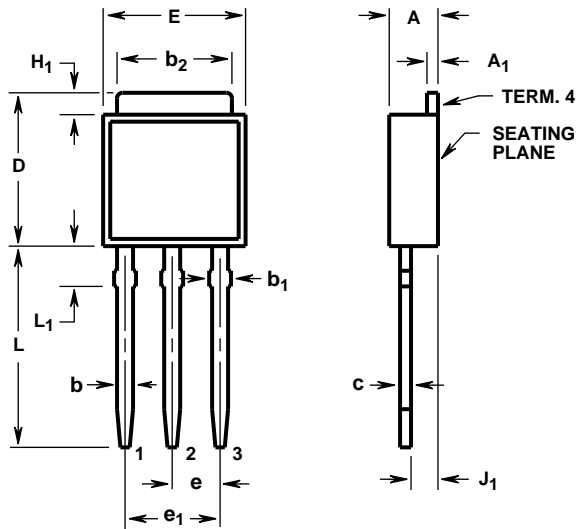
$f_{MAX1}$  is defined by  $f_{MAX1} = 0.05 / (t_{D(OFF)I} + t_{D(ON)I})$ . Dead-time (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible.  $t_{D(OFF)I}$  and  $t_{D(ON)I}$  are defined in Figure 19.

Device turn-off delay can establish an additional frequency limiting condition for an application other than  $T_{JMAX}$ .  $t_{D(OFF)I}$  is important when controlling output ripple under a lightly loaded condition.

$f_{MAX2}$  is defined by  $f_{MAX2} = (P_D - P_C) / (E_{OFF} + E_{ON})$ . The allowable dissipation ( $P_D$ ) is defined by  $P_D = (T_{JMAX} - T_C) / R_{\theta JC}$ . The sum of device switching and conduction losses must not exceed  $P_D$ . A 50% duty factor was used (Figure 13) and the conduction losses ( $P_C$ ) are approximated by  $P_C = (V_{CE} \times I_{CE}) / 2$ .  $E_{ON}$  and  $E_{OFF}$  are defined in the switching waveforms shown in Figure 19.  $E_{ON}$  is the integral of the instantaneous power loss ( $I_{CE} \times V_{CE}$ ) during turn-on and  $E_{OFF}$  is the integral of the instantaneous power loss ( $I_{CE} \times V_{CE}$ ) during turn-off. All tail losses are included in the calculation for  $E_{OFF}$ ; i.e. the collector current equals zero ( $I_{CE} = 0$ ).

HGTD7N60C3, HGTD7N60C3S, HGTP7N60C3

Packaging



LEAD #	TERMINAL
1	Gate
2	Collector
3	Emitter
Term. 4	Collector

TO-251AA

3 LEAD JEDEC TO-251AA PLASTIC PACKAGE

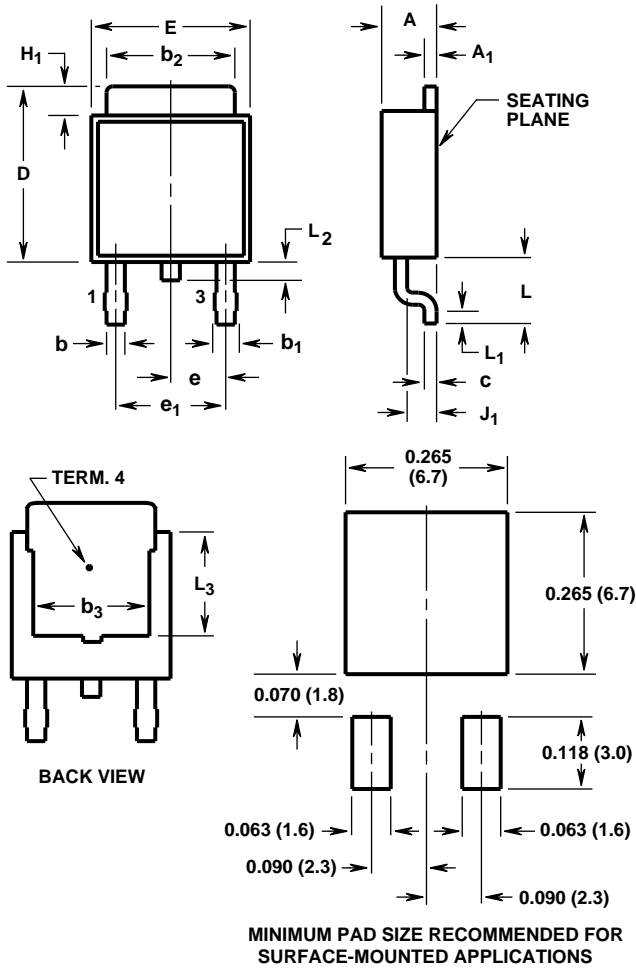
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A <sub>1</sub>	0.018	0.022	0.46	0.55	3, 4
b	0.028	0.032	0.72	0.81	3, 4
b <sub>1</sub>	0.033	0.040	0.84	1.01	3
b <sub>2</sub>	0.205	0.215	5.21	5.46	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		5
e <sub>1</sub>	0.180 BSC		4.57 BSC		5
H <sub>1</sub>	0.035	0.045	0.89	1.14	-
J <sub>1</sub>	0.040	0.045	1.02	1.14	6
L	0.355	0.375	9.02	9.52	-
L <sub>1</sub>	0.075	0.090	1.91	2.28	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-251AA outline dated 9-88.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 10-95.

HGTD7N60C3, HGTD7N60C3S, HGTP7N60C3

Packaging (Continued)



LEAD #	TERMINAL
1	Gate
3	Emitter
Term. 4	Collector

TO-252AA

SURFACE MOUNT JEDEC TO-252AA PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A <sub>1</sub>	0.018	0.022	0.46	0.55	4, 5
b	0.028	0.032	0.72	0.81	4, 5
b <sub>1</sub>	0.033	0.040	0.84	1.01	4
b <sub>2</sub>	0.205	0.215	5.21	5.46	4, 5
b <sub>3</sub>	0.190	-	4.83	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		7
e <sub>1</sub>	0.180 BSC		4.57 BSC		7
H <sub>1</sub>	0.035	0.045	0.89	1.14	-
J <sub>1</sub>	0.040	0.045	1.02	1.14	-
L	0.100	0.115	2.54	2.92	-
L <sub>1</sub>	0.020	-	0.51	-	4, 6
L <sub>2</sub>	0.025	0.040	0.64	1.01	3
L <sub>3</sub>	0.170	-	4.32	-	2

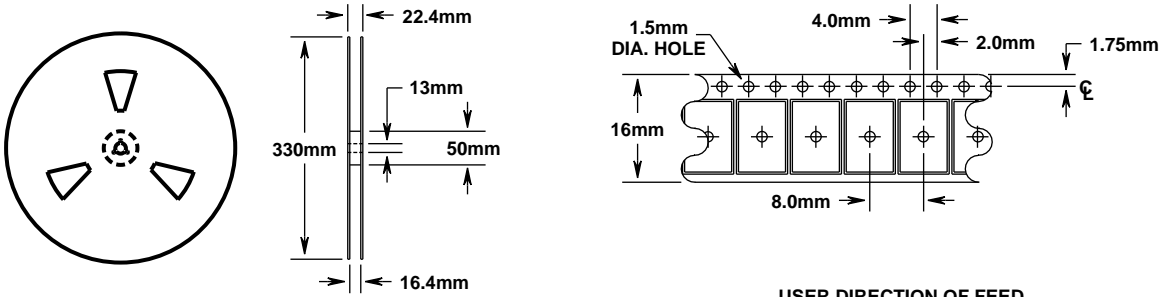
NOTES:

1. These dimensions are within allowable dimensions of Rev. B of JEDEC TO-252AA outline dated 9-88.
2. L<sub>3</sub> and b<sub>3</sub> dimensions establish a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L<sub>1</sub> is the terminal length for soldering.
7. Position of lead to be measured 0.090 inches (2.28mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 5 dated 10-95.

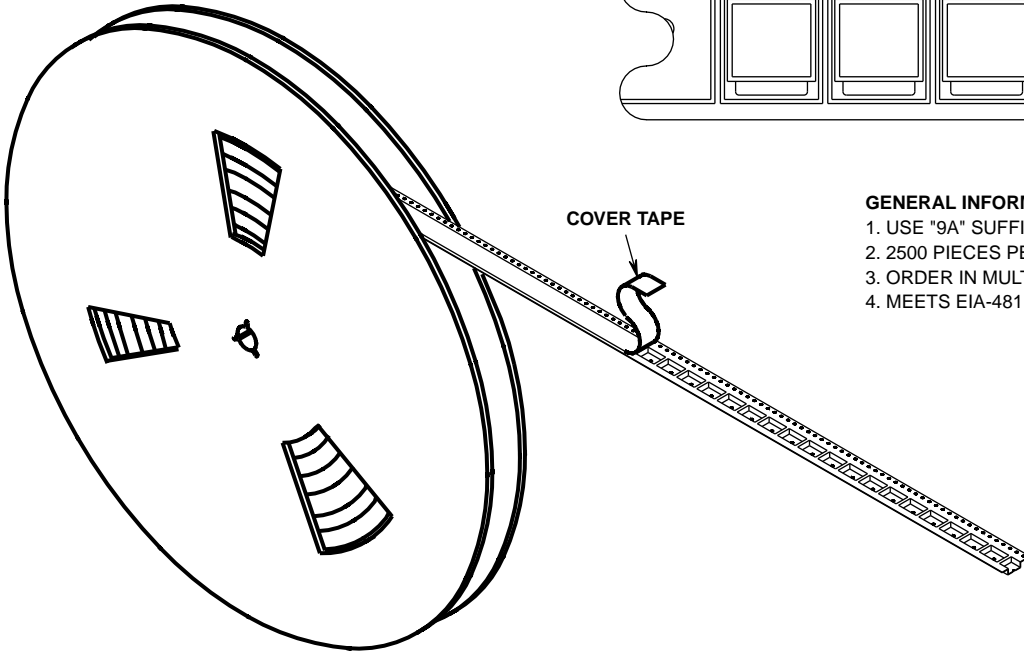
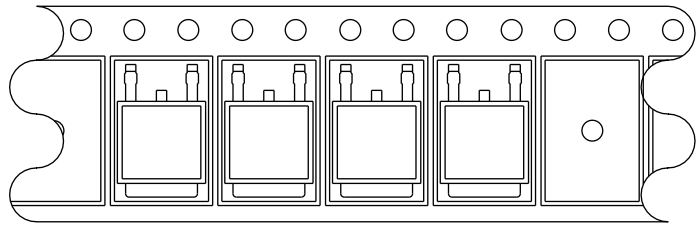


**Packaging** (Continued)

**TO-252AA**  
16mm TAPE AND REEL



USER DIRECTION OF FEED



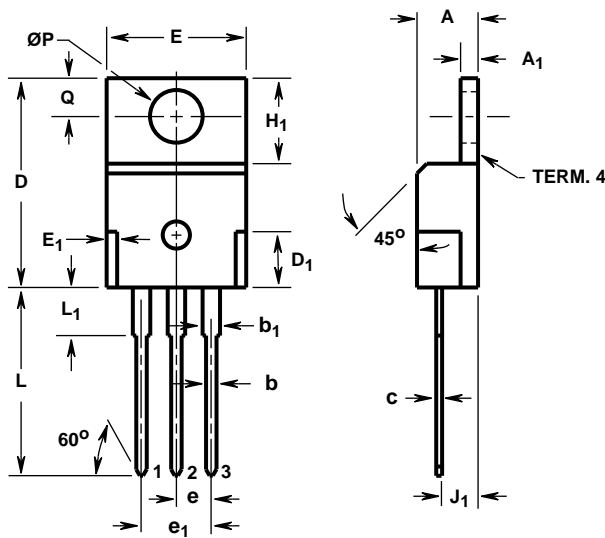
**GENERAL INFORMATION**

1. USE "9A" SUFFIX ON PART NUMBER.
2. 2500 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 5 dated 10-95

# HGTD7N60C3, HGTD7N60C3S, HGTP7N60C3

## Packaging (Continued)



LEAD #	TERMINAL
1	Gate
2	Collector
3	Emitter
Term. 4	Collector

## TO-220AB

### 3 LEAD JEDEC TO-220AB PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A <sub>1</sub>	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b <sub>1</sub>	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D <sub>1</sub>	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E <sub>1</sub>	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e <sub>1</sub>	0.200 BSC		5.08 BSC		5
H <sub>1</sub>	0.235	0.255	5.97	6.47	-
J <sub>1</sub>	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L <sub>1</sub>	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

#### NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L<sub>1</sub>.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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## Sales Office Headquarters

For general information regarding Harris Semiconductor and its products, call **1-800-4-HARRIS**

### NORTH AMERICA

Harris Semiconductor  
P. O. Box 883, Mail Stop 53-210  
Melbourne, FL 32902  
TEL: 1-800-442-7747  
(407) 729-4984  
FAX: (407) 729-5321

### EUROPE

Harris Semiconductor  
Mercure Center  
100, Rue de la Fusee  
1130 Brussels, Belgium  
TEL: (32) 2.724.2111  
FAX: (32) 2.724.22.05

### ASIA

Harris Semiconductor PTE Ltd.  
No. 1 Tannery Road  
Cencon 1, #09-01  
Singapore 1334  
TEL: (65) 748-4200  
FAX: (65) 748-0400

