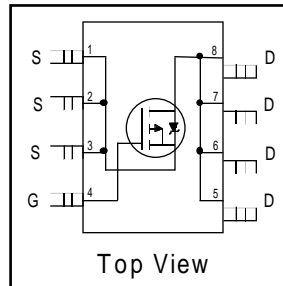


## HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- P-Channel MOSFET
- Very Small SOIC Package
- Low Profile (<1.1mm)
- Available in Tape & Reel
- Fast Switching

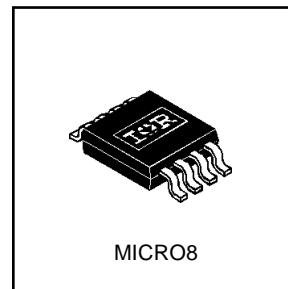


|                           |
|---------------------------|
| $V_{DSS} = -30V$          |
| $R_{DS(on)} = 0.09\Omega$ |

### Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The new Micro8 package, with half the footprint area of the standard SO-8, provides the smallest footprint available in an SOIC outline. This makes the Micro8 an ideal device for applications where printed circuit board space is at a premium. The low profile (<1.1mm) of the Micro8 will allow it to fit easily into extremely thin application environments such as portable electronics and PCMCIA cards.



### Absolute Maximum Ratings

|                          | Parameter                                 | Max.         | Units |
|--------------------------|---|--------------|-------|
| $I_D @ T_A = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ -10V$ | -3.6         | A     |
| $I_D @ T_A = 70^\circ C$ | Continuous Drain Current, $V_{GS} @ -10V$ | -2.9         |       |
| $I_{DM}$                 | Pulsed Drain Current ①                    | -19          |       |
| $P_D @ T_A = 25^\circ C$ | Power Dissipation                         | 1.8          | W     |
|                          | Linear Derating Factor                    | 14           | mW/°C |
| $V_{GS}$                 | Gate-to-Source Voltage                    | $\pm 20$     | V     |
| $dv/dt$                  | Peak Diode Recovery $dv/dt$ ②             | -5.0         | V/ns  |
| $T_J, T_{STG}$           | Junction and Storage Temperature Range    | -55 to + 150 | °C    |

### Thermal Resistance Ratings

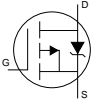
|                 | Parameter                     | Typ. | Max. | Units |
|-----------------|-------------------------------|------|------|-------|
| $R_{\theta JA}$ | Maximum Junction-to-Ambient ④ | —    | 70   | °C/W  |

All Micro8 Data Sheets reflect improved Thermal Resistance, Power and Current -Handling Ratings- effective only for product marked with Date Code 505 or later .

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

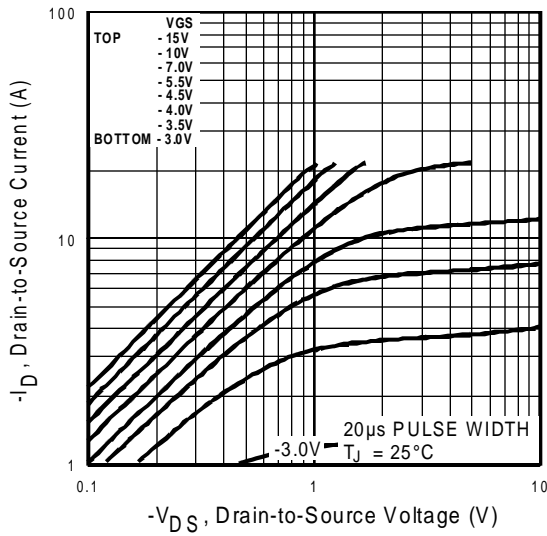
|                                 | Parameter                            | Min. | Typ.  | Max. | Units               | Conditions  |
|---------------------------------|--------------------------------------|------|-------|------|---------------------|---|
| $V_{(BR)DSS}$                   | Drain-to-Source Breakdown Voltage    | -30  | —     | —    | V                   | $V_{GS} = 0V, I_D = -250\mu A$                        |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient  | —    | 0.024 | —    | V/ $^\circ\text{C}$ | Reference to $25^\circ\text{C}$ , $I_D = -1mA$        |
| $R_{DS(on)}$                    | Static Drain-to-Source On-Resistance | —    | —     | 0.09 | $\Omega$            | $V_{GS} = -10V, I_D = -2.4A$ ③                        |
|                                 |                                      | —    | —     | 0.15 |                     | $V_{GS} = -4.5V, I_D = -1.2A$ ③                       |
| $V_{GS(th)}$                    | Gate Threshold Voltage               | -1.0 | —     | —    | V                   | $V_{DS} = V_{GS}, I_D = -250\mu A$                    |
| $g_{fs}$                        | Forward Transconductance             | 2.3  | —     | —    | S                   | $V_{DS} = -10V, I_D = -1.2A$                          |
| $I_{DSS}$                       | Drain-to-Source Leakage Current      | —    | —     | -1.0 | $\mu A$             | $V_{DS} = -24V, V_{GS} = 0V$                          |
|                                 |                                      | —    | —     | -25  |                     | $V_{DS} = -24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$ |
| $I_{GSS}$                       | Gate-to-Source Forward Leakage       | —    | —     | -100 | nA                  | $V_{GS} = -20V$                                       |
|                                 | Gate-to-Source Reverse Leakage       | —    | —     | 100  |                     | $V_{GS} = 20V$  |
| $Q_g$                           | Total Gate Charge                    | —    | 20    | 30   | nC                  | $I_D = -2.4A$   |
| $Q_{gs}$                        | Gate-to-Source Charge                | —    | 2.1   | 3.1  |                     | $V_{DS} = -24V$                                       |
| $Q_{gd}$                        | Gate-to-Drain ("Miller") Charge      | —    | 7.6   | 11   |                     | $V_{GS} = -10V$ , See Fig. 6 and 9 ③                  |
| $t_{d(on)}$                     | Turn-On Delay Time                   | —    | 13    | —    | ns                  | $V_{DD} = -15V$                                       |
| $t_r$                           | Rise Time                            | —    | 20    | —    |                     | $I_D = -2.4A$   |
| $t_{d(off)}$                    | Turn-Off Delay Time                  | —    | 43    | —    |                     | $R_G = 6.2\Omega$                                     |
| $t_f$                           | Fall Time                            | —    | 39    | —    |                     | $R_D = 6.2\Omega$ , See Fig. 10 ③                     |
| $C_{iss}$                       | Input Capacitance                    | —    | 520   | —    |                     | $V_{GS} = 0V$   |
| $C_{oss}$                       | Output Capacitance                   | —    | 300   | —    | pF                  | $V_{DS} = -25V$                                       |
| $C_{rss}$                       | Reverse Transfer Capacitance         | —    | 140   | —    |                     | $f = 1.0MHz$ , See Fig. 5                             |

## Source-Drain Ratings and Characteristics

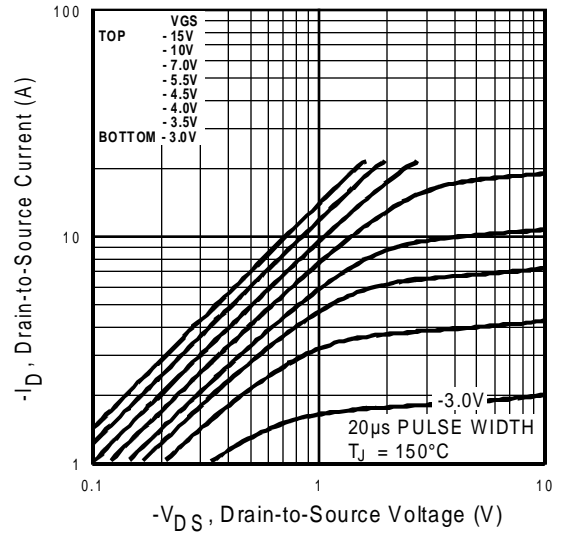
|          | Parameter                                 | Min. | Typ. | Max. | Units | Conditions   |
|----------|---|------|------|------|-------|--|
| $I_S$    | Continuous Source Current<br>(Body Diode) | —    | —    | -1.8 | A     | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current<br>(Body Diode) ①   | —    | —    | -19  |       |  |
| $V_{SD}$ | Diode Forward Voltage                     | —    | —    | -1.2 | V     | $T_J = 25^\circ\text{C}, I_S = -2.4A, V_{GS} = 0V$ ③   |
| $t_{rr}$ | Reverse Recovery Time                     | —    | 43   | 64   | ns    | $T_J = 25^\circ\text{C}, I_F = -2.4A$  |
| $Q_{rr}$ | Reverse Recovery Charge                   | —    | 50   | 76   | nC    | $di/dt = -100A/\mu s$ ③  |

### Notes:

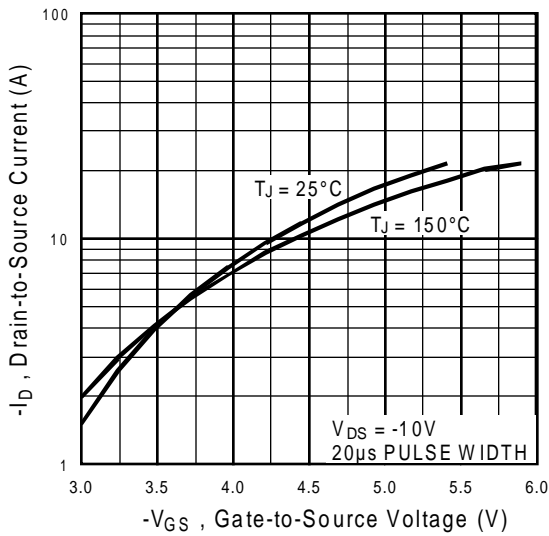
- ① Repetitive rating – pulse width limited by max. junction temperature (see fig. 11)
- ②  $I_{SD} \leq -2.4A, di/dt \leq -130A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
- ③ Pulse width  $\leq 300\mu s$  – duty cycle  $\leq 2\%$
- ④ Surface mounted on FR-4 board,  $t \leq 10sec.$



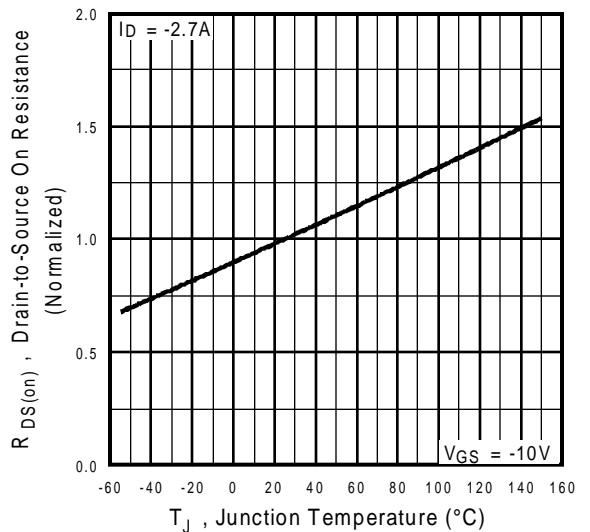
**Fig 1.** Typical Output Characteristics



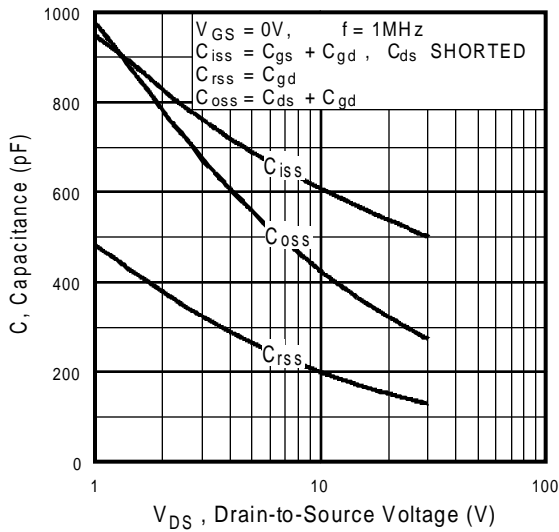
**Fig 2.** Typical Output Characteristics



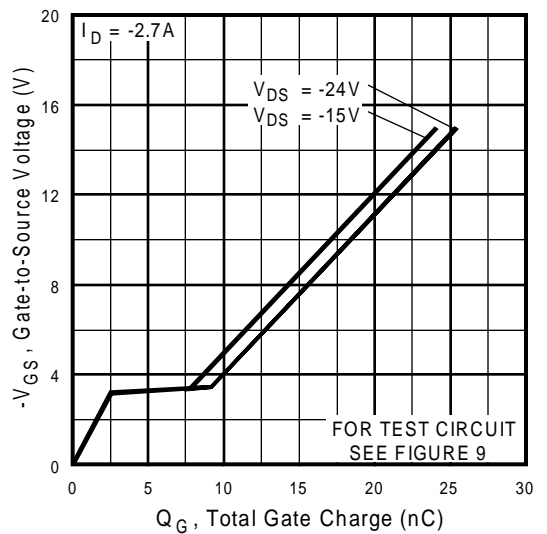
**Fig 3.** Typical Transfer Characteristics



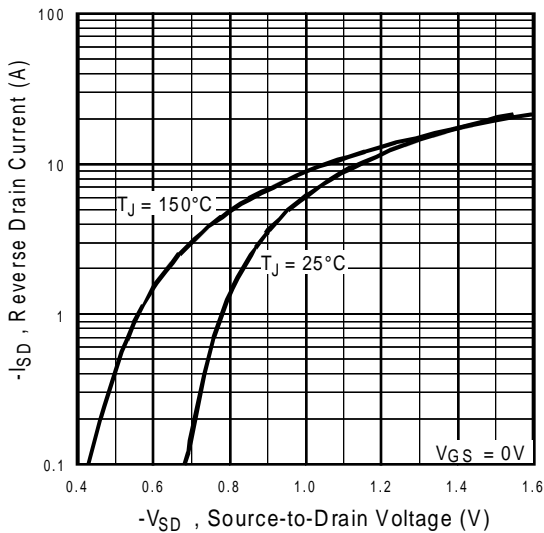
**Fig 4.** Normalized On-Resistance Vs. Temperature



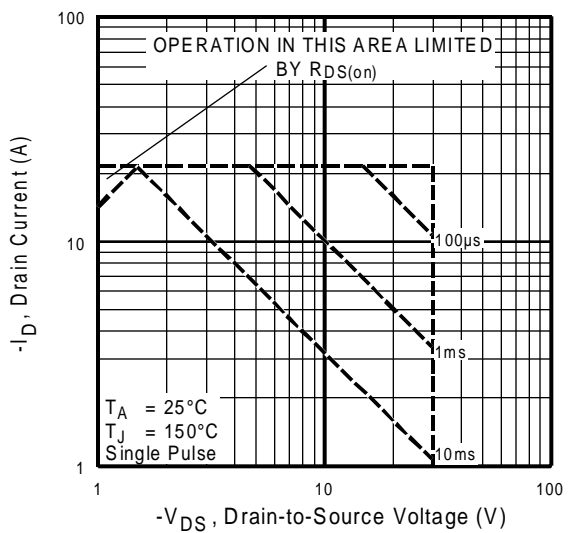
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

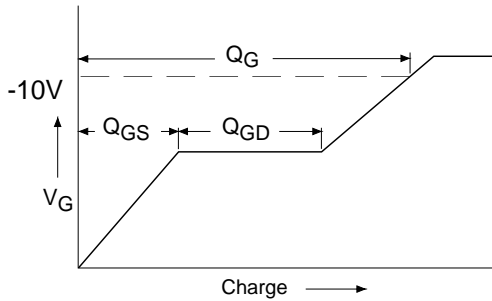


Fig 9a. Basic Gate Charge Waveform

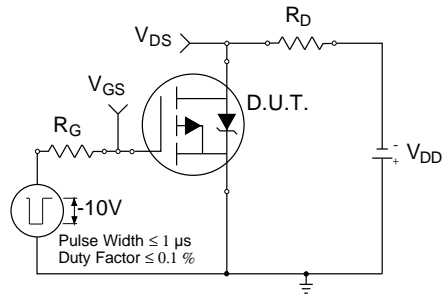


Fig 10a. Switching Time Test Circuit

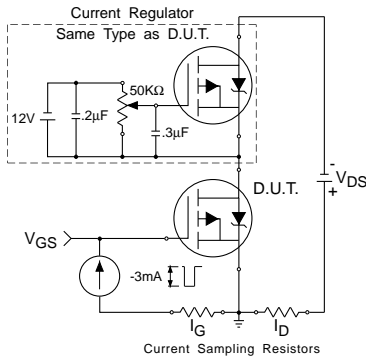


Fig 9b. Gate Charge Test Circuit

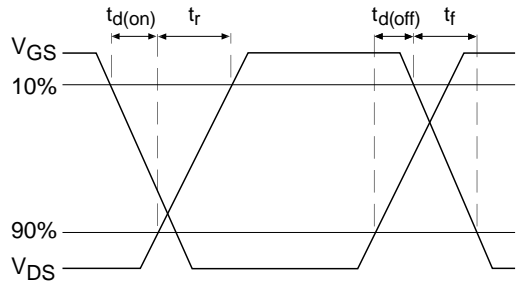


Fig 10b. Switching Time Waveforms

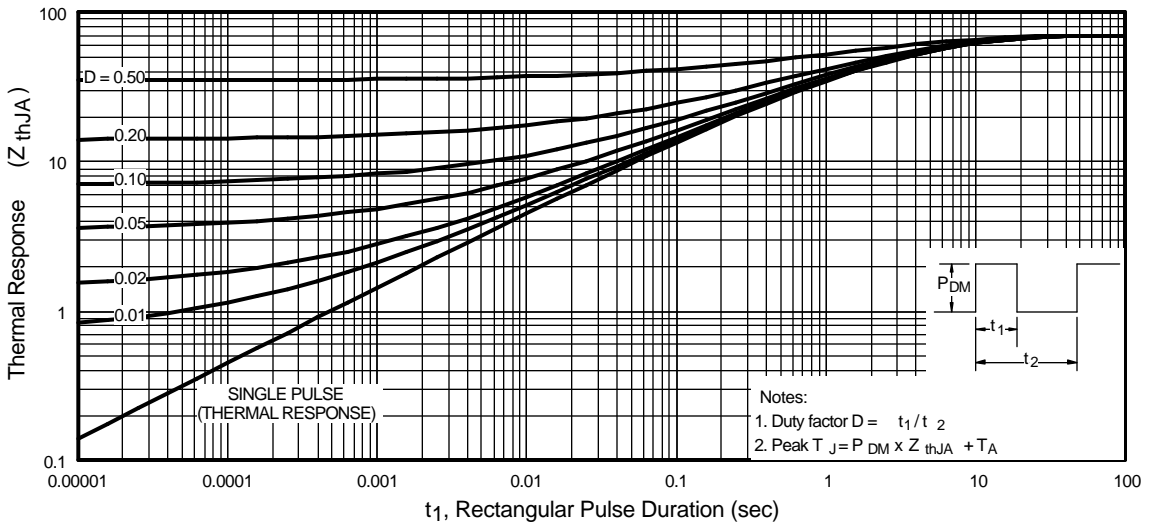
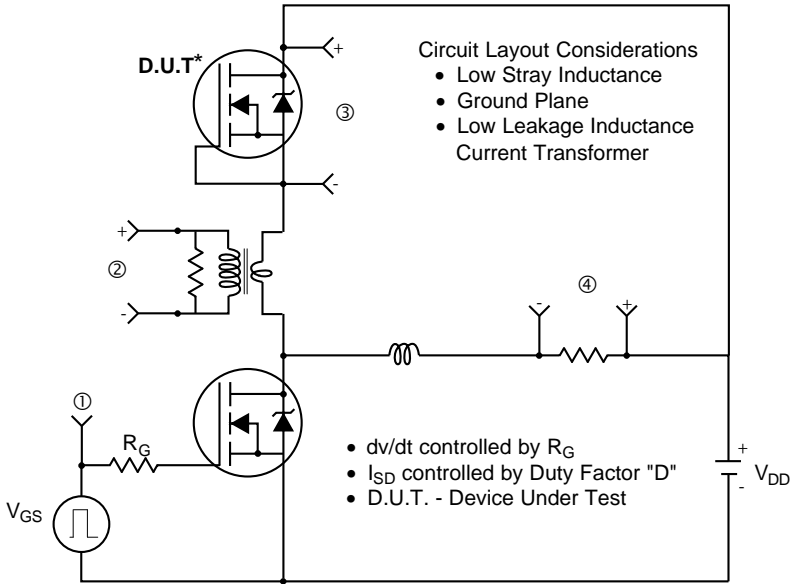
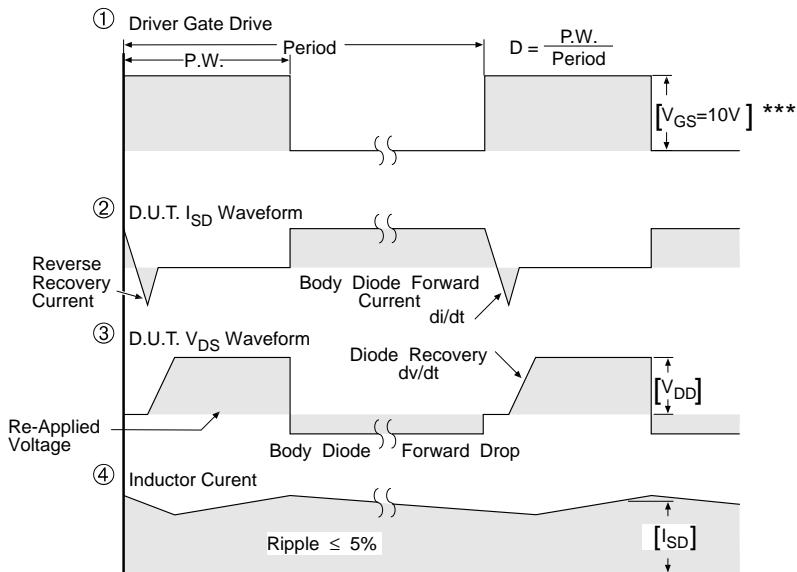


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity of D.U.T for P-Channel



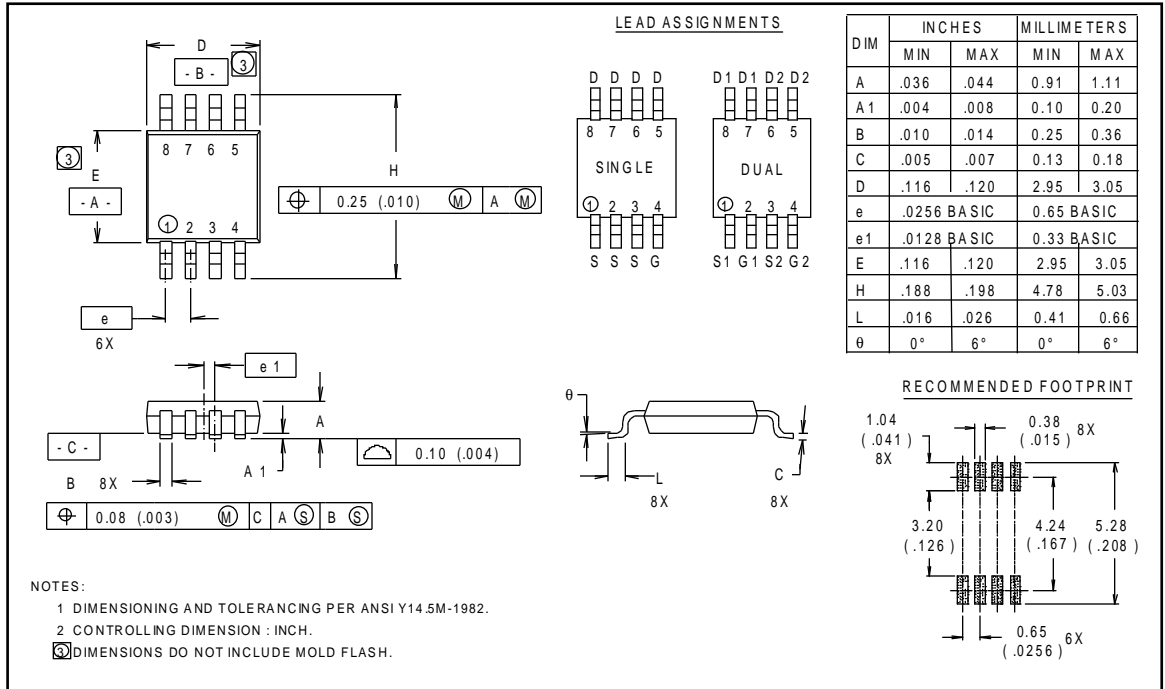
\*\*\*  $V_{GS} = 5.0V$  for Logic Level and  $3V$  Drive Devices

**Fig 12.** For P-Channel HEXFETS

## Package Outline

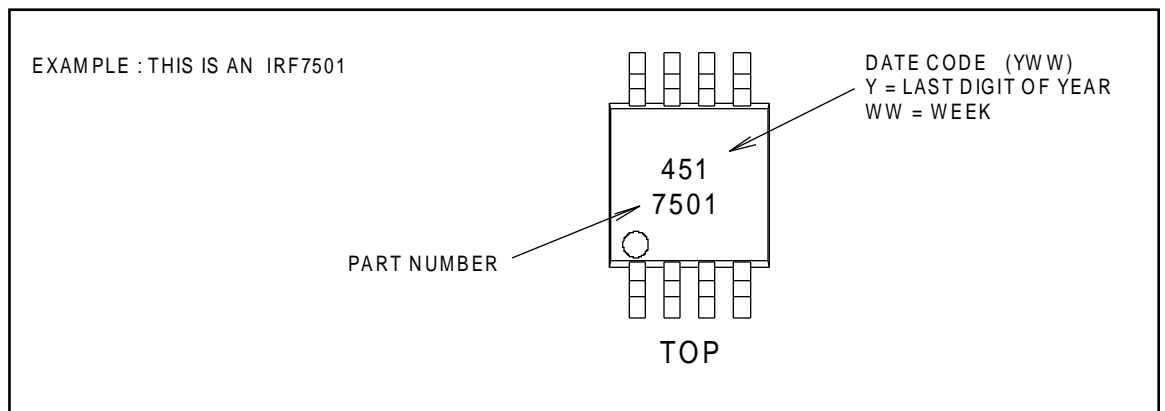
### Micro8 Outline

Dimensions are shown in millimeters (inches)



## Part Marking Information

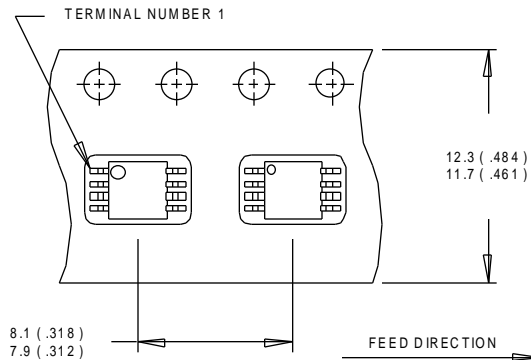
### Micro8



## Tape & Reel Information

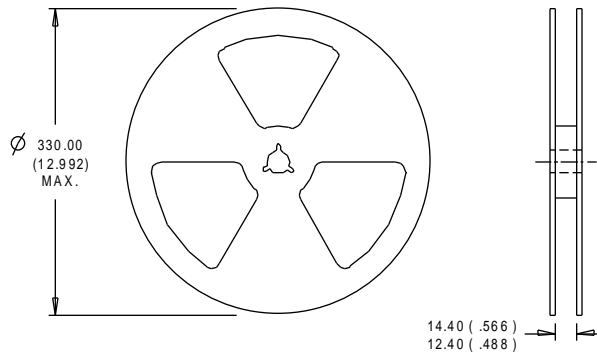
### Micro8

Dimensions are shown in millimeters (inches)



**NOTES:**

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.
2. CONTROLLING DIMENSION : MILLIMETER.



**NOTES :**

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