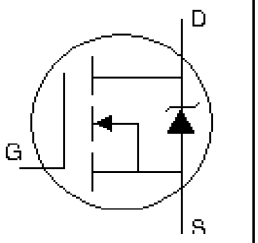
International
IOR Rectifier

PD - 9.1222

IRFI1310G

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Isolated Package
- High Voltage Isolation = 2.5KVRMS⑤
- Sink to Lead Creepage Dist. = 4.8mm
- Repetitive Avalanche Rated
- 175°C Operating Temperature



V_{DSS} = 100V

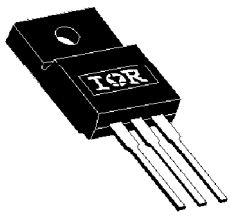
$R_{DS(on)}$ = 0.04Ω

I_D = 22A

Description

Fourth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



TO-220 FULLPAK

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	22	
I_D @ T_C = 100°C	Continuous Collector Current, V_{GS} @ 10V	15	A
I_{DM}	Pulsed Drain Current ①	88	
P_D @T_C = 25°C	Power Dissipation	48	W
	Linear Derating Factor	0.32	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	120	mJ
I_{AR}	Avalanche Current ①	22	A
E_{AR}	Repetitive Avalanche Energy ①	4.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

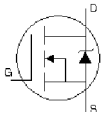
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	——	3.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient		——	——	65

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	——	——	V	V_{GS} = 0V, ID = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.10	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	——	——	0.04	Ω	V_{GS} = 10V, I_D = 13A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	12	——	——	S	V_{DS} = 50V, I_D = 25A
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	µA	V_{DS} = 100V, V_{GS} = 0V
		——	——	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
Q_g	Total Gate Charge	——	——	110	nC	I_D = 25A
Q_{gs}	Gate-to-Source Charge	——	——	18		V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	42		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	——	13	——	ns	V_{DD} = 50V
t_r	Rise Time	——	77	——		I_D = 25A
$t_{d(off)}$	Turn-Off Delay Time	——	82	——		R_G = 9.1Ω
t_f	Fall Time	——	64	——		R_D = 2.0Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	——	7.5	——		
C_{iss}	Input Capacitance	——	2500	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	630	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	130	——		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	22	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	88		
V_{SD}	Diode Forward Voltage	——	——	2.5	V	T_J = 25°C, I_S = 13A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	140	210	ns	T_J = 25°C, I_F = 25A
Q_{rr}	Reverse RecoveryCharge	——	0.79	1.2	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 25V, starting T_J = 25°C, L = 1.0mH R_G = 25Ω, I_{AS} = 13A. (See Figure 12)

③ I_{SD} ≤ 25A, di/dt ≤ 170A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ t=60s, f=60Hz

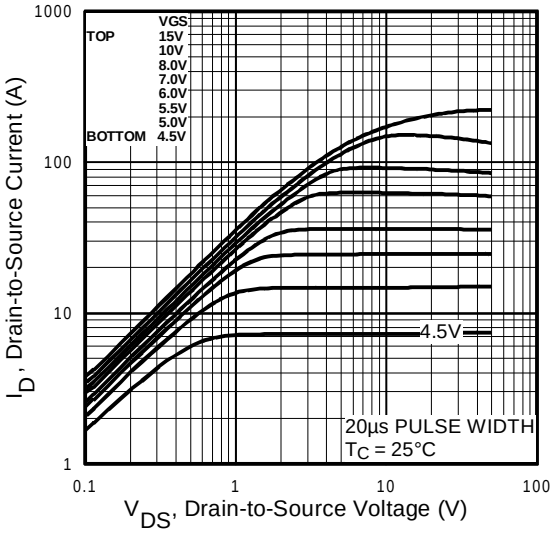


Fig 1. Typical Output Characteristics, $T_C = 25^oC$

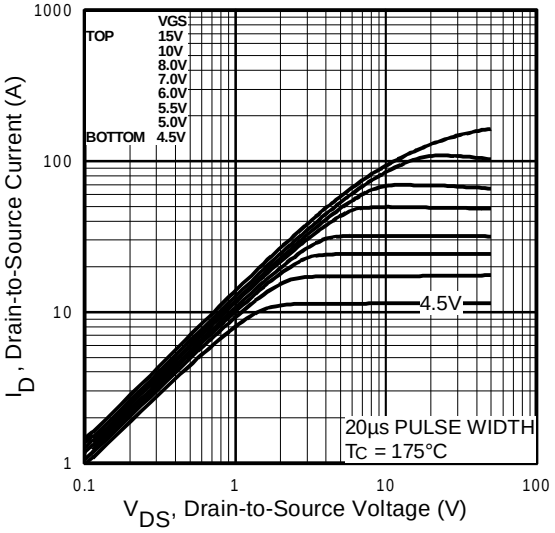


Fig 2. Typical Output Characteristics, $T_C = 175^oC$

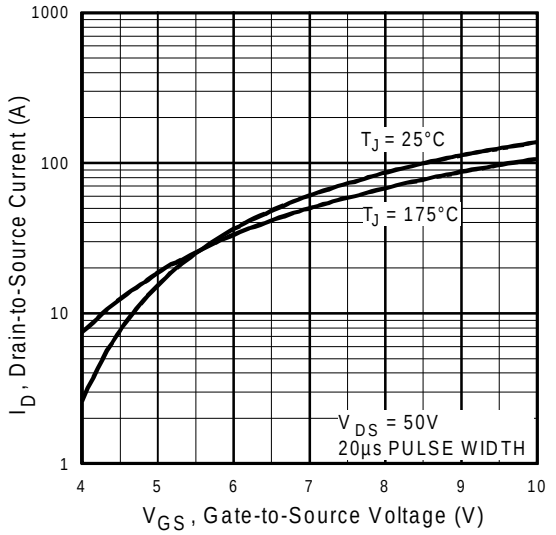


Fig 3. Typical Transfer Characteristics

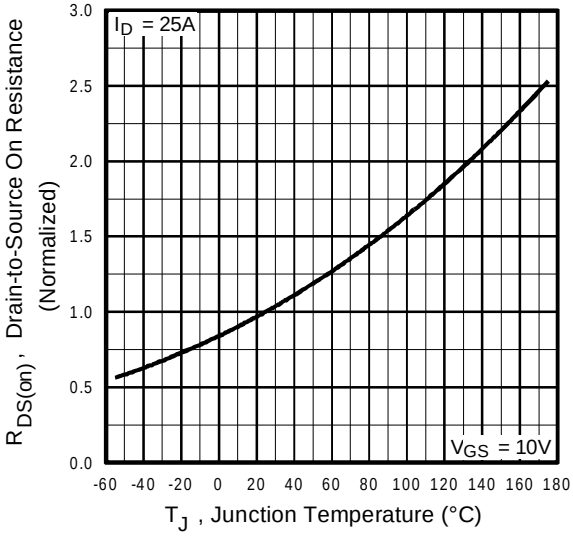


Fig 4. Normalized On-Resistance Vs. Temperature

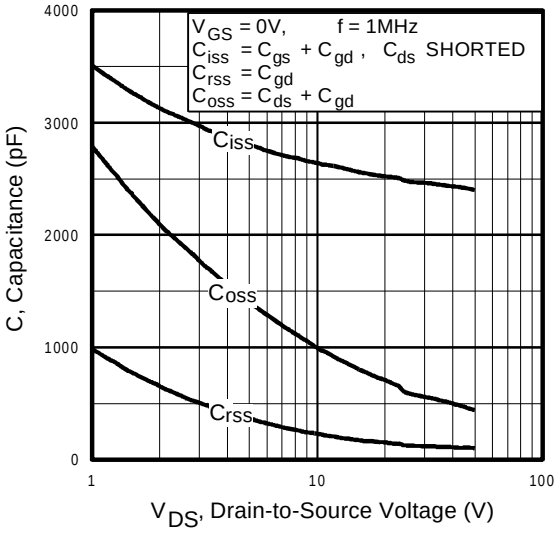


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

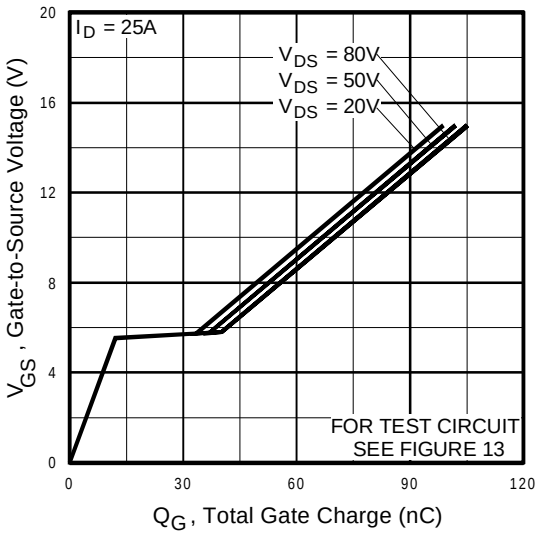


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

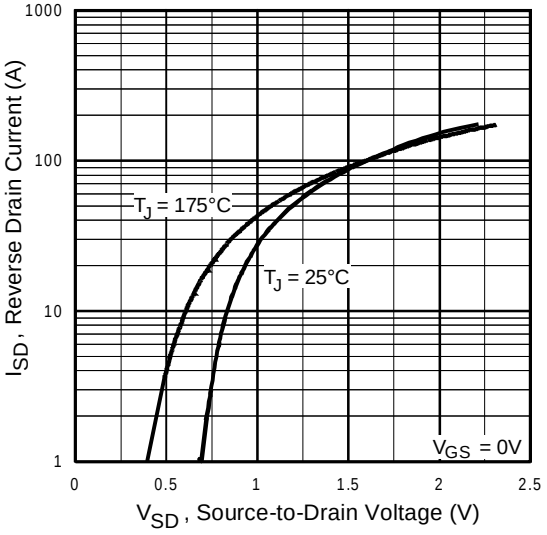


Fig 7. Typical Source-Drain Diode Forward Voltage

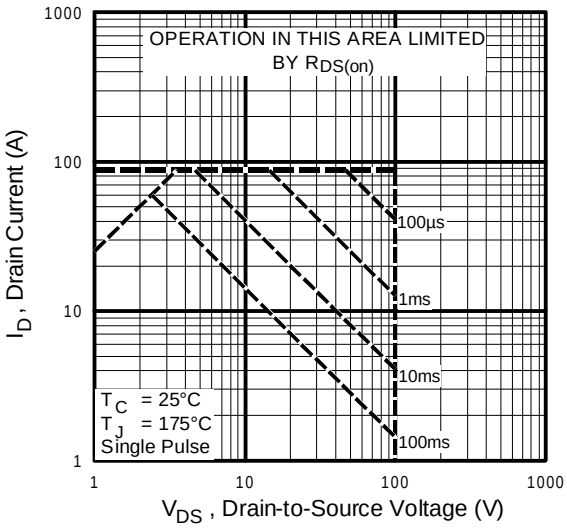


Fig 8. Maximum Safe Operating Area

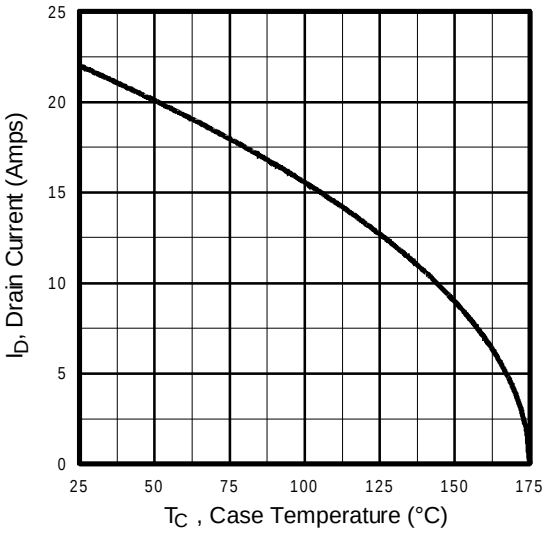


Fig 9. Maximum Drain Current Vs. Case Temperature

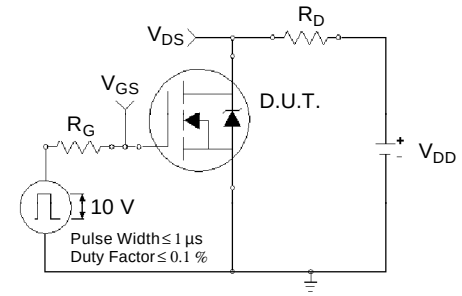


Fig 10a. Switching Time Test Circuit

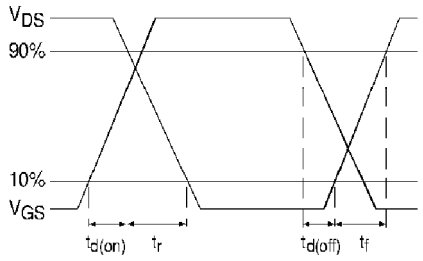


Fig 10b. Switching Time Waveforms

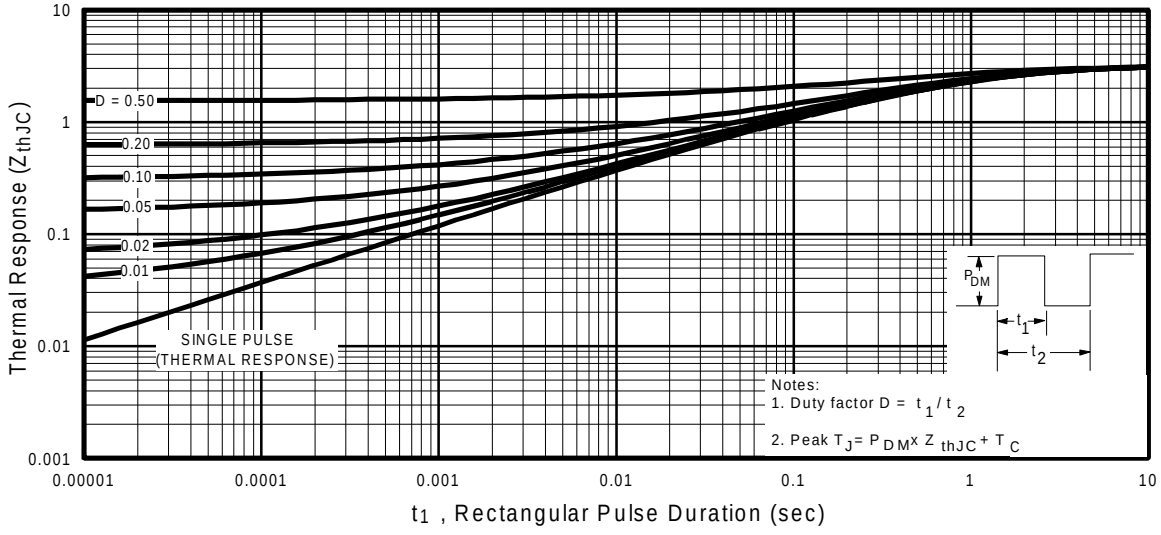


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

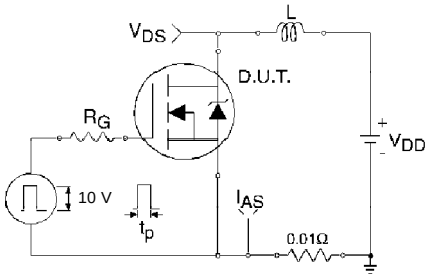


Fig 12a. Unclamped Inductive Test Circuit

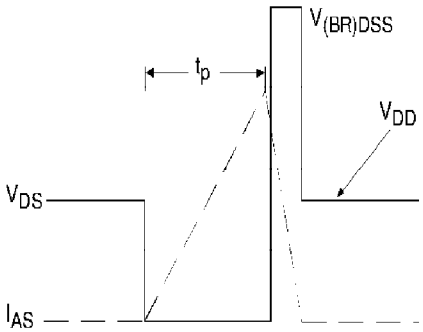


Fig 12b. Unclamped Inductive Waveforms

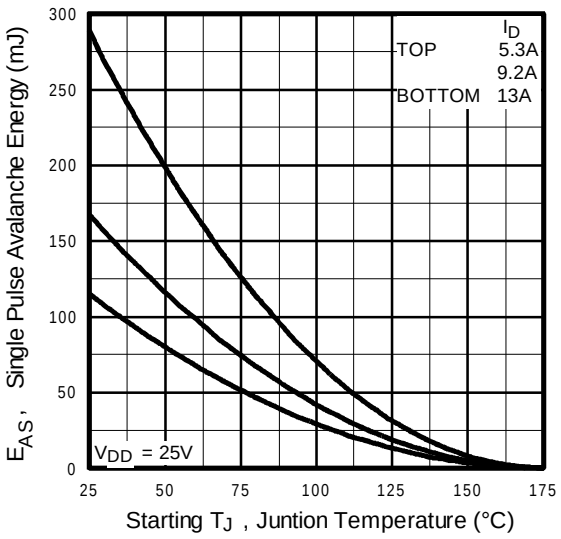


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

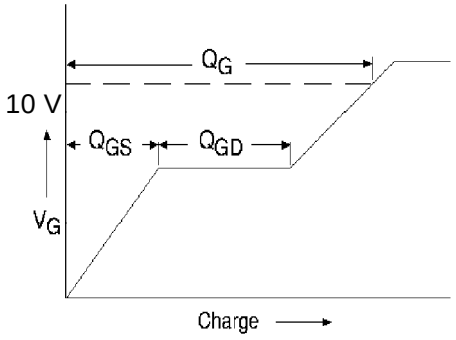


Fig 13a. Basic Gate Charge Waveform

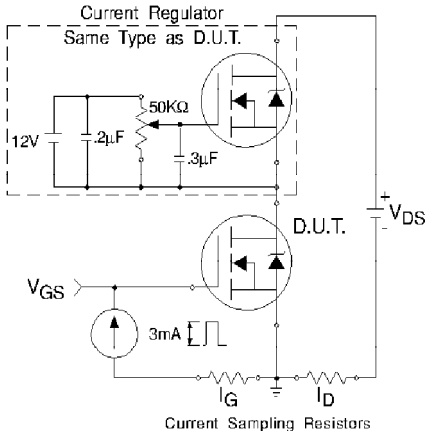


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit

Appendix B: Package Outline Mechanical Drawing

Appendix C: Part Marking Information

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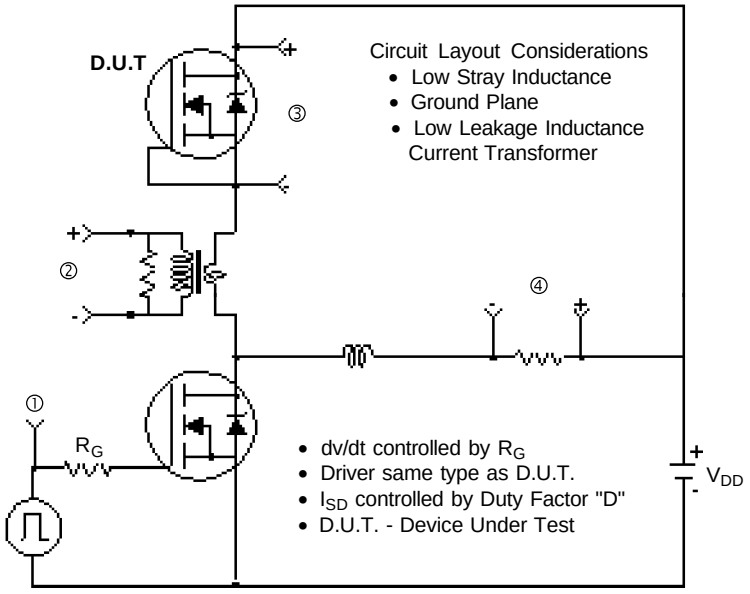
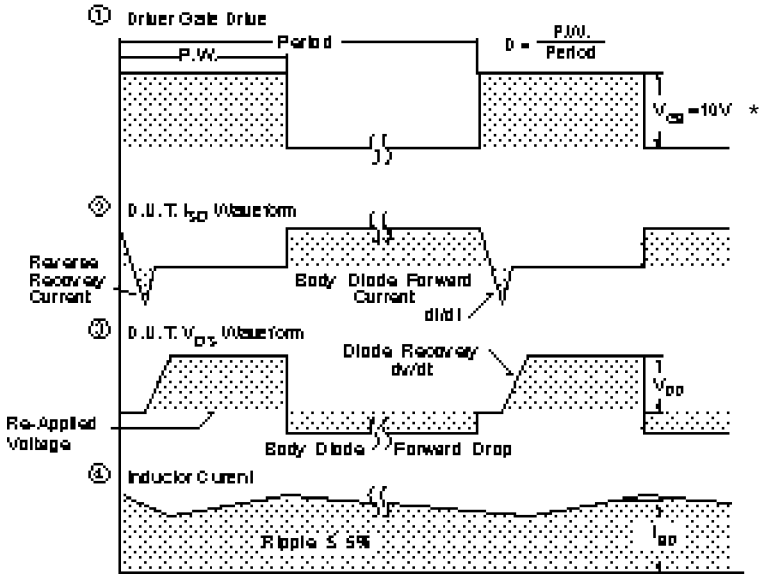
Peak Diode Recovery dv/dt Test Circuit



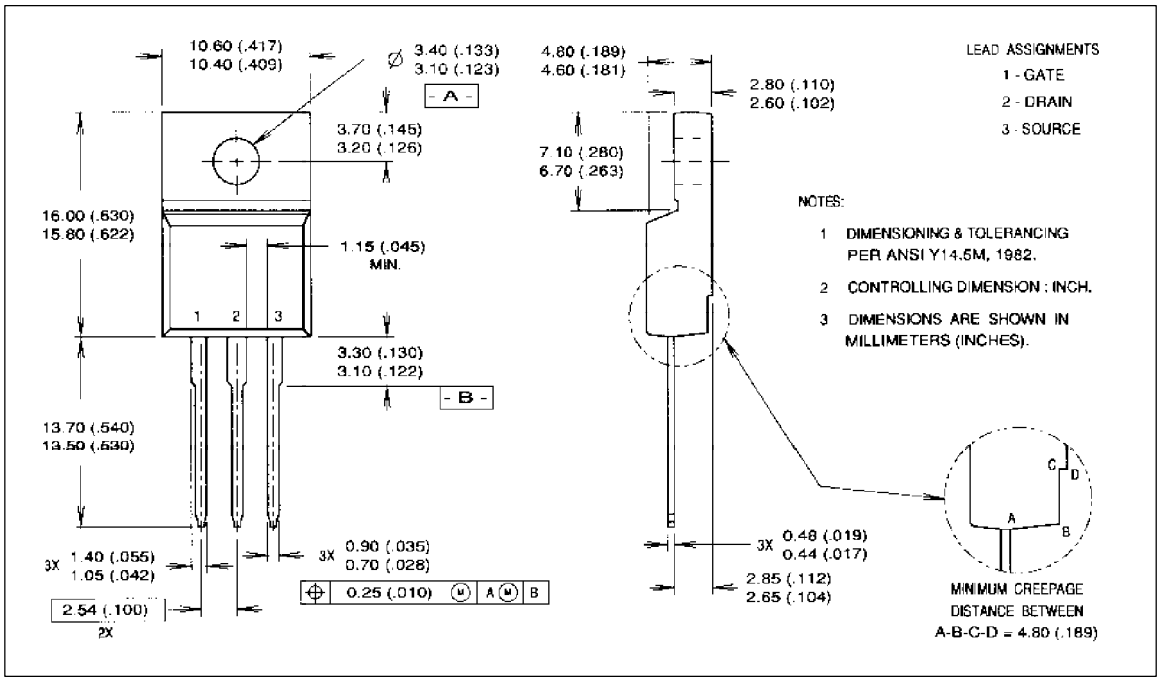


* VGS = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

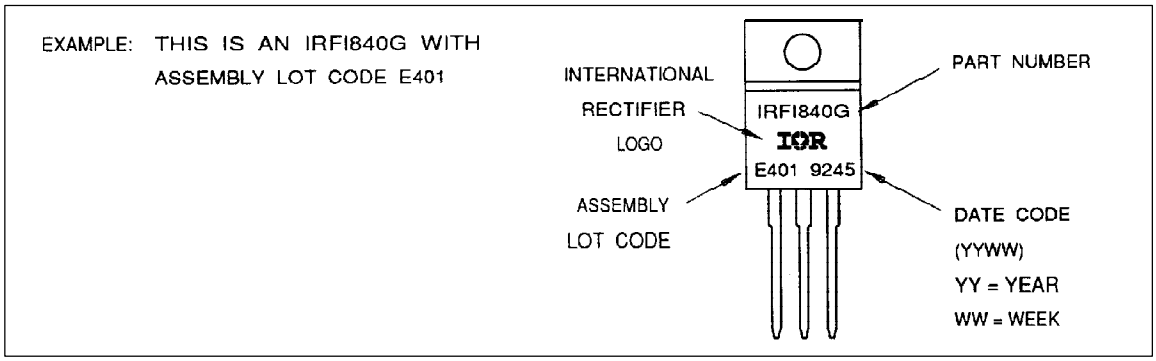
Package Outline

TO-220 Full-Pak



Part Marking Information

TO-220 Full-Pak



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