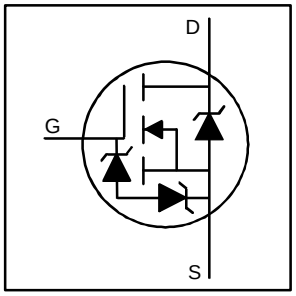
PD - 9.1253

# International IOR Rectifier

# IRFR2605
# IRFU2605

HEXFET® Power MOSFET

- Ultra Low On-Resistance
- ESD Protected
- Surface Mount (IRFR2605)
- Straight Lead (IRFU2605)
- 150°C Operating Temperature
- Repetitive Avalanche Rated
- Fast Switching




$V_{DSS}$ = 55V

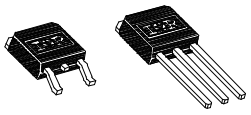
$R_{DS(on)}$ = 0.075Ω

$I_D$ = 19A

## Description

Fourth Generation HEXFETs from International Rectifier utilize advanced processing techniques that achieve extremely low on-resistance per silicon area and allow electrostatic discharge protection to be integrated in the gate structure. These benefits, combined with the ruggedized device design that HEXFETs are known for, provide the designer with extremely efficient and reliable device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



D-PAK TO-252AA I-PAK TO-251AA

## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 19 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V | 12 | |
| $I_{DM}$ | Pulsed Drain Current ① | 76 | |
| $P_D$ @$T_C$ = 25°C | Power Dissipation | 50 | W |
| $P_D$ @$T_C$ = 25°C | Power Dissipation (PCB Mount)** | 3.1 | |
| | Linear Derating Factor | 0.40 | W/°C |
| | Linear Derating Factor (PCB Mount)** | 0.025 | |
| $V_{GS}$ | Gate-to-Source Voltage | ±20 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy ② | 100 | mJ |
| $I_{AR}$ | Avalanche Current ① | 12 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | 5.0 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 4.5 | V/ns |
| $T_J$, $T_{STG}$ | Junction and Storage Temperature Range | -55 to + 150 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |
| $V_{ESD}$ | Human Body Model, 100pF, 1.5KΩ | 2000 | V |

## Thermal Resistance

| | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | — | — | 2.5 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount)** | — | — | 40 | |
| $R_{\theta JA}$ | Junction-to-Ambient | — | — | 62 | |

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 55 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.051 | — | V/°C | Reference to 25°C, $I_D$ = 1mA |
| $R_{DS(ON)}$ | Static Drain-to-Source On-Resistance | — | — | 0.085 | Ω | $V_{GS}$ = 10V, $I_D$ = 11A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| $g_{fs}$ | Forward Transconductance | 3.6 | — | — | S | $V_{DS}$ = 25V, $I_D$ = 11A |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 25 | µA | $V_{DS}$ = 55V, $V_{GS}$ = 0V |
| | | — | — | 250 | | $V_{DS}$ = 44V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 10 | µA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | — | — | -10 | | $V_{GS}$ = -20V |
| $Q_g$ | Total Gate Charge | — | — | 23 | nC | $I_D$ = 11A |
| $Q_{gs}$ | Gate-to-Source Charge | — | — | 5.4 | | $V_{DS}$ = 44V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | — | — | 10 | | $V_{GS}$ = 10V, See Fig. 6 and 13 ④ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 7.1 | — | ns | $V_{DD}$ = 25V |
| $t_r$ | Rise Time | — | 56 | — | | $I_D$ = 11A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 31 | — | | $R_G$ = 20Ω |
| $t_f$ | Fall Time | — | 39 | — | | $R_D$ = 2.2Ω, See Fig. 10 ④ |
| $L_D$ | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| $L_S$ | Internal Source Inductance | — | 7.5 | — | | |
| $C_{iss}$ | Input Capacitance | — | 420 | — | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | — | 250 | — | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 67 | — | | $f$ = 1.0MHz, See Fig. 5 |

## Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 18 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | — | — | 72 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.5 | V | $T_J$ = 25°C, $I_S$ = 11A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | — | 67 | 100 | ns | $T_J$ = 25°C, $I_F$ = 11A |
| $Q_{rr}$ | Reverse RecoveryCharge | — | 0.18 | 0.26 | µC | di/dt = 100A/µs ④ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$+$L_D$) | | | | |

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )

② $V_{DD}$ = 25V, starting $T_J$ = 25°C, L = 830µH $R_G$ = 25Ω, $I_{AS}$ = 11A. (See Figure 12)

③ $I_{SD}$ ≤ 11A, di/dt ≤ 110A/µs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ ≤ 150°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

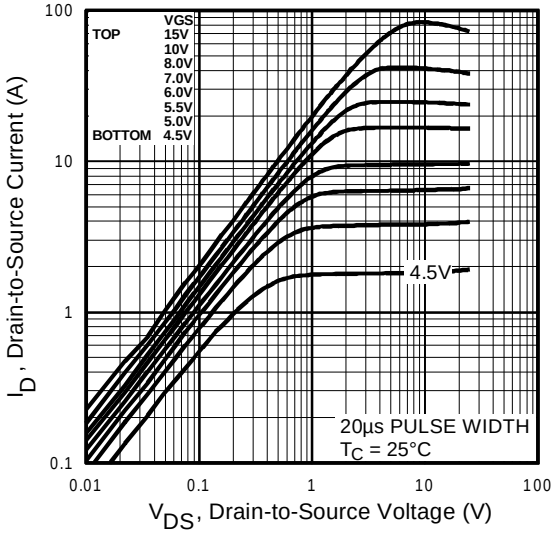



**Fig 1.** Typical Output Characteristics, $T_C = 25^oC$

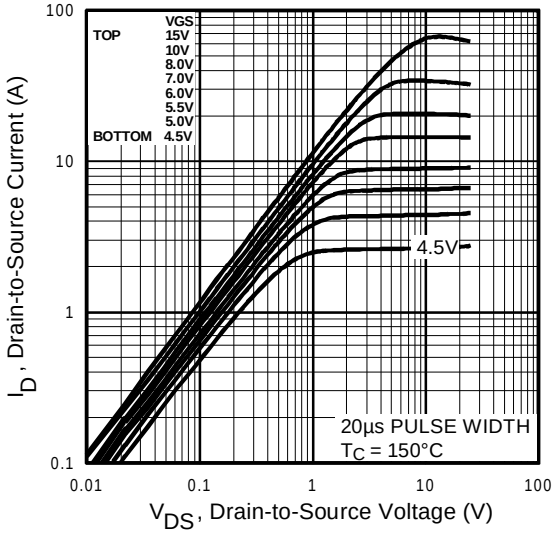



**Fig 2.** Typical Output Characteristics, $T_C = 150^oC$

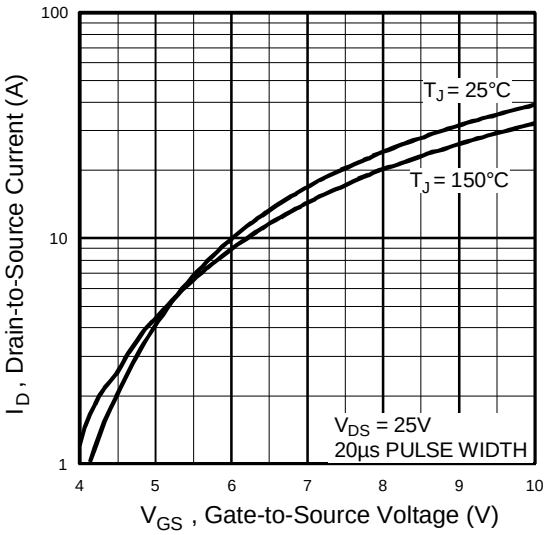



**Fig 3.** Typical Transfer Characteristics

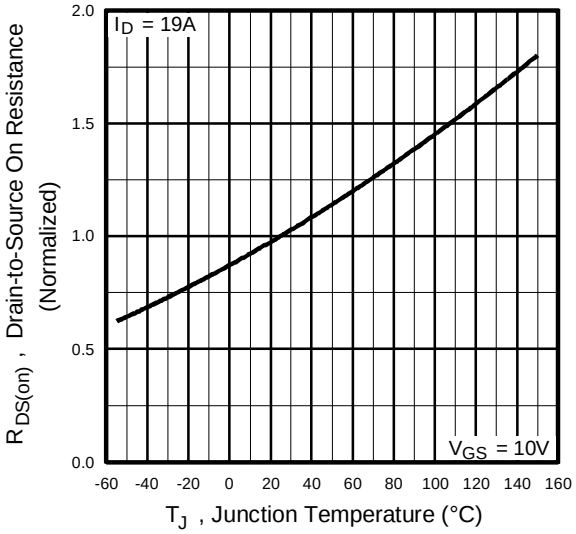



**Fig 4.** Normalized On-Resistance Vs. Temperature

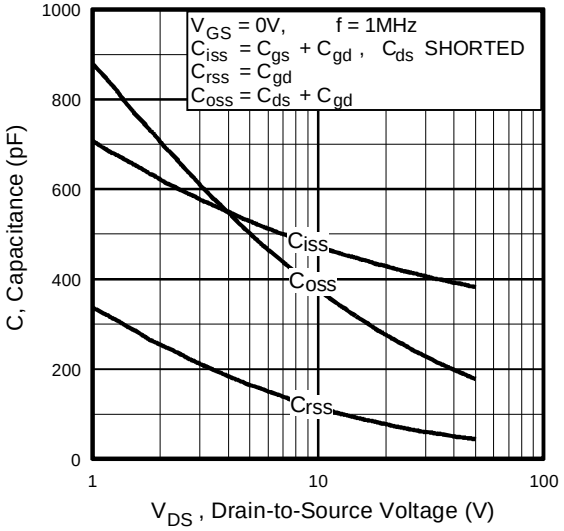



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

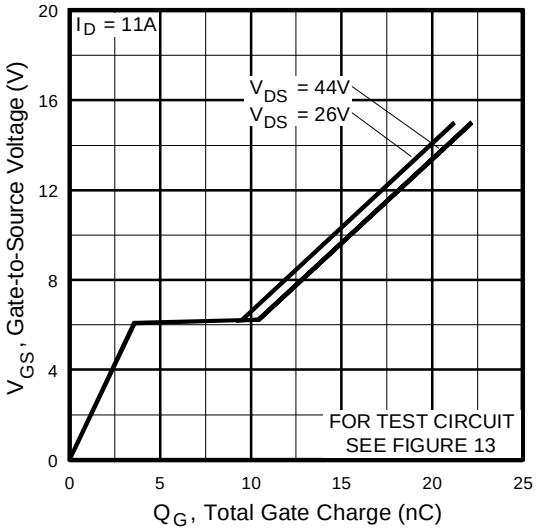



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

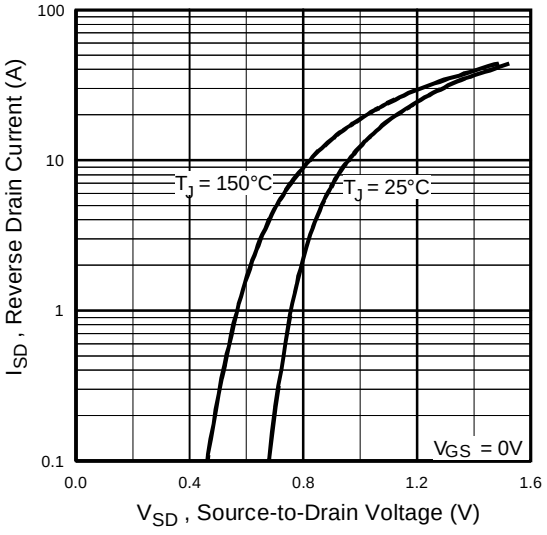



**Fig 7.** Typical Source-Drain Diode Forward Voltage

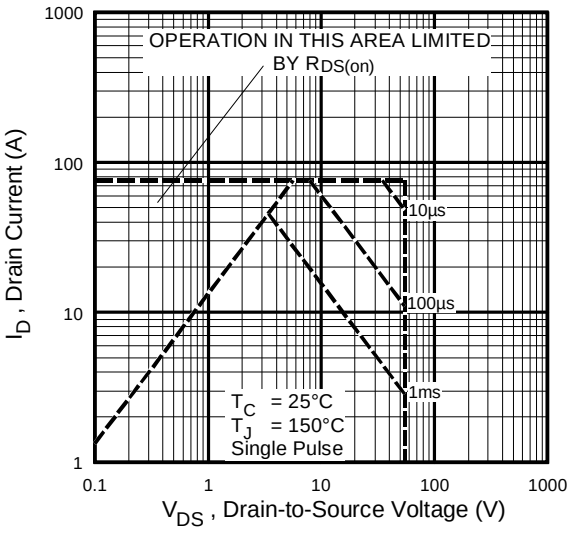



**Fig 8.** Maximum Safe Operating Area

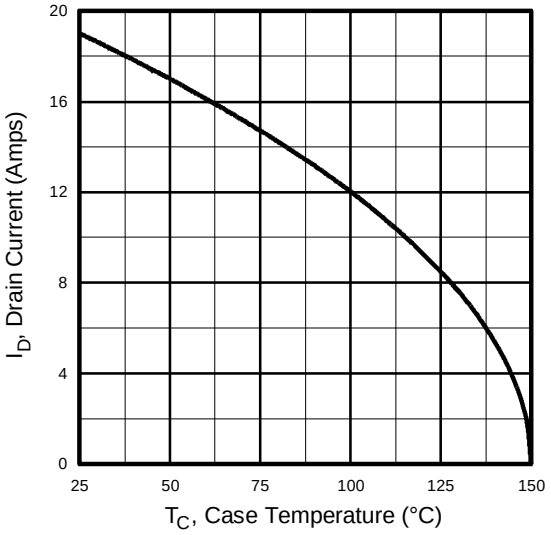



**Fig 9.** Maximum Drain Current Vs. Case Temperature

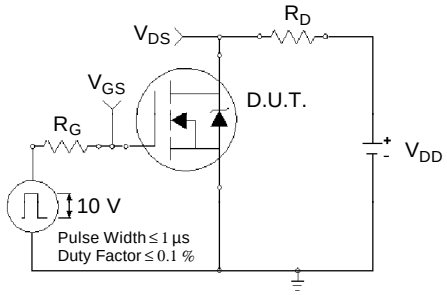



**Fig 10a.** Switching Time Test Circuit

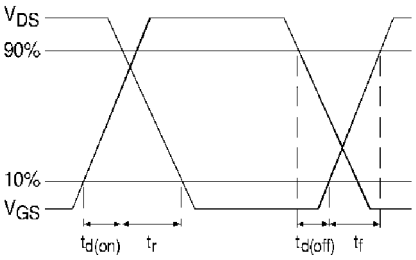



**Fig 10b.** Switching Time Waveforms

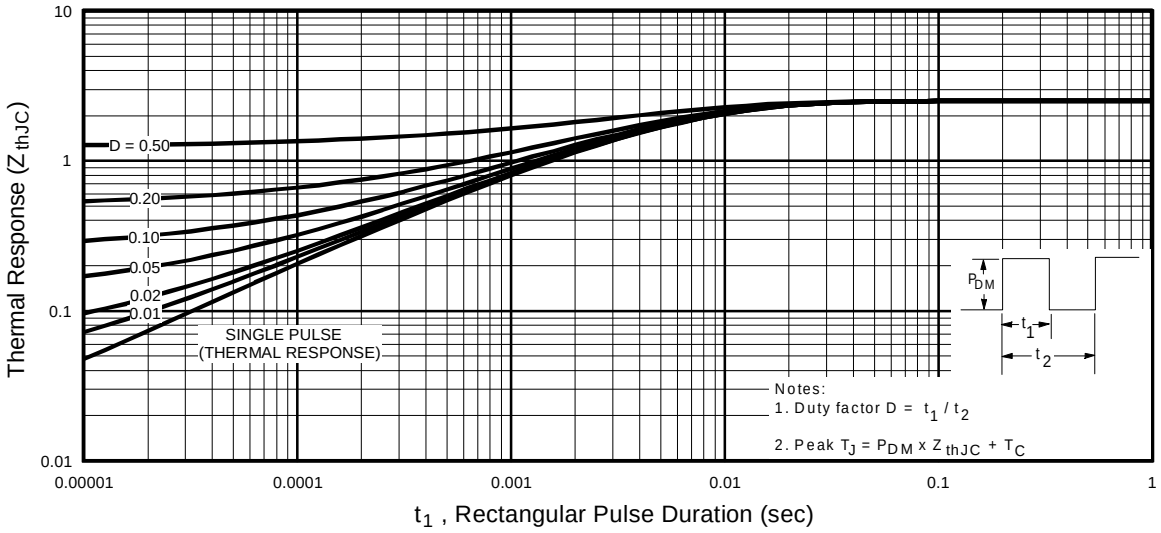



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

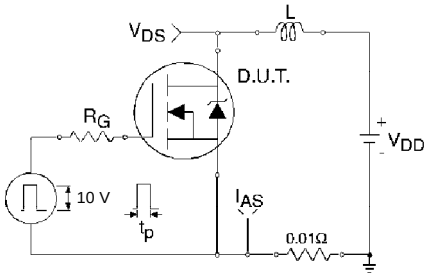



**Fig 12a.** Unclamped Inductive Test Circuit

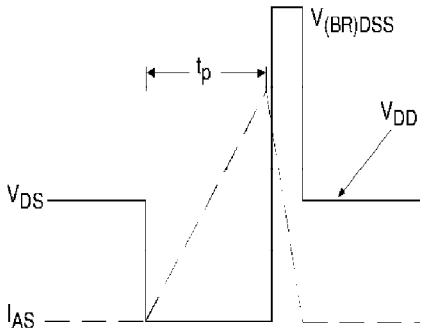



**Fig 12b.** Unclamped Inductive Waveforms

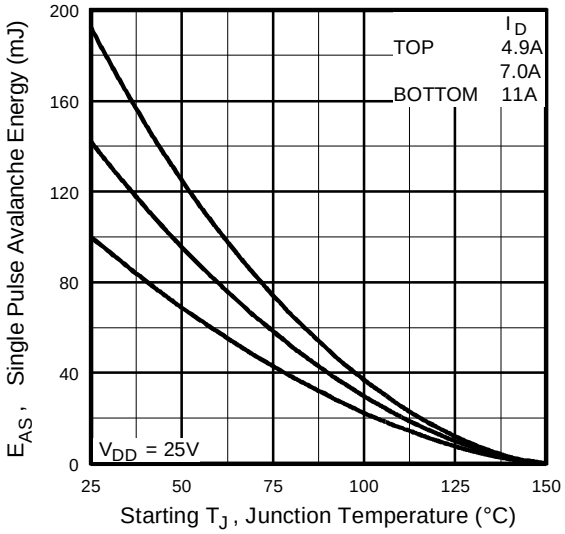



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

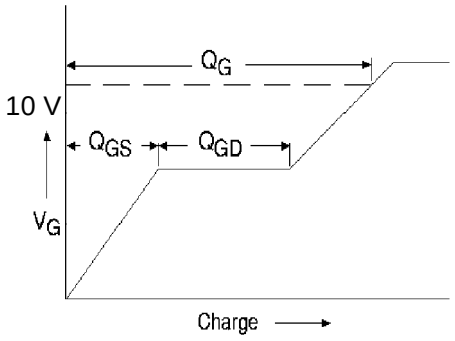



**Fig 13a.** Basic Gate Charge Waveform

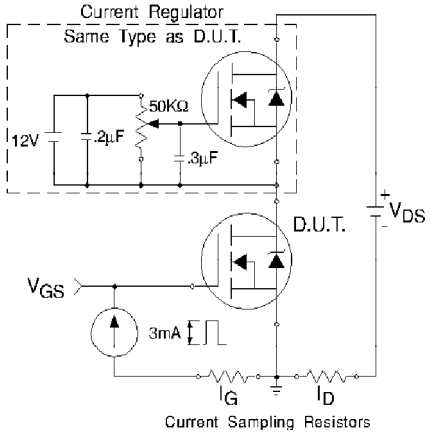
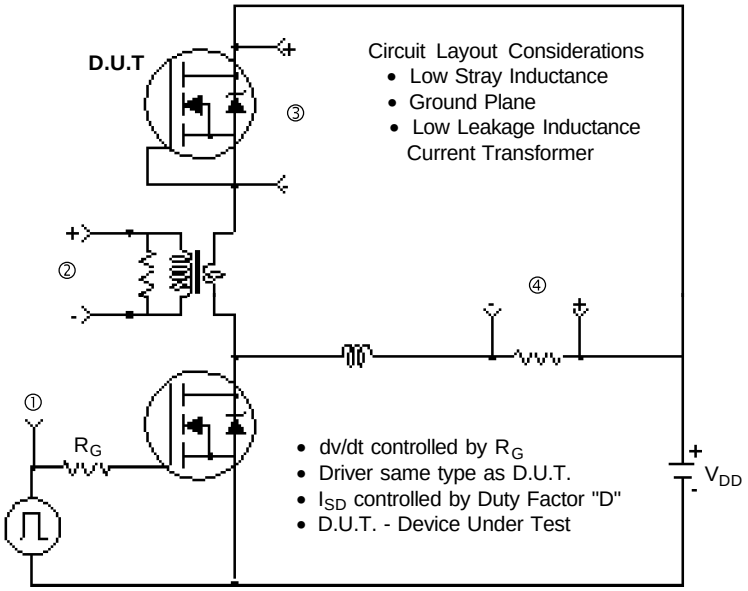
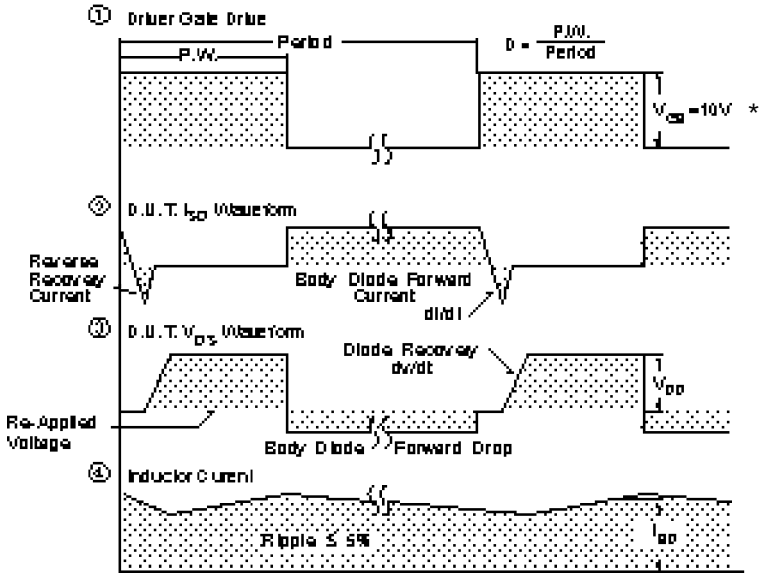



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



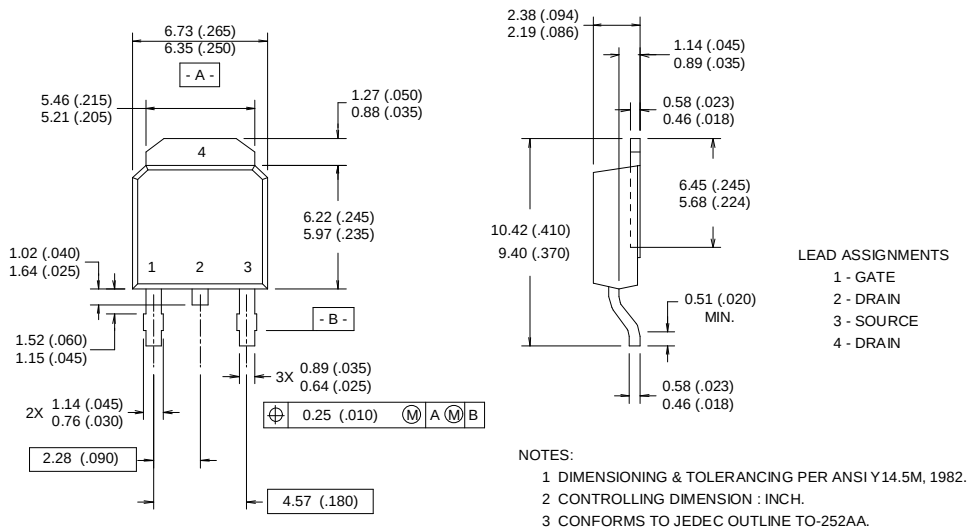

* VGS = 5V for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

## Package Outline

**D-PAK Outline**

Dimensions are shown in millimeters (inches)



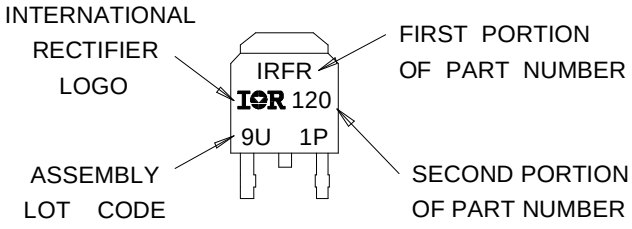

NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

## Part Marking Information

**D-PAK**

EXAMPLE : THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P




**WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
**EUROPEAN HEADQUARTERS:** Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: (44) 0883 713215
**IR CANADA:** 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 3L1, Tel: (905) 475 1897 **IR GERMANY:** Saalburgstrasse 157, 61350 Bad Homburg Tel: 6172 37066 **IR ITALY:** Via Liguria 49, 10071 Borgaro, Torino Tel: (39) 1145 10111 **IR FAR EAST:** K&H Bldg., 2F, 3-30-4 Nishi-Ikeburo 3-Chome, Toshima-Ki, Tokyo 171 Tel: (03)3983 0641 **IR SOUTHEAST ASIA:** 315 Outram Road, #10-02 Tan Boon Liat Building, 0316 Tel: 65 221 8371