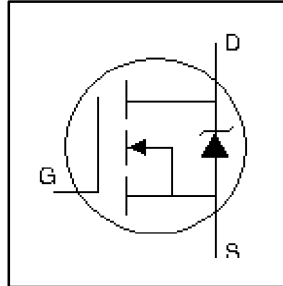


HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation = 2.5KVRMS^⑤
- Sink to Lead Creepage Dist. 4.8mm
- Logic-Level Gate Drive
- $R_{DS(ON)}$ Specified at $V_{GS} = 4V$ & $5V$
- Fast Switching
- Ease of paralleling



$$V_{DSS} = 200V$$

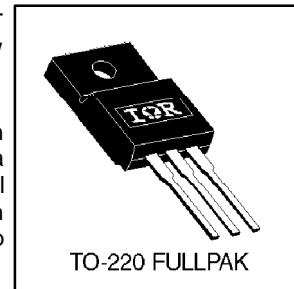
$$R_{DS(on)} = 0.18\Omega$$

$$I_D = 9.9A$$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 5.0V	9.9	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, V_{GS} @ 5.0V	6.3	
I_{DM}	Pulsed Drain Current ①	40	
P_D @ $T_C = 25^\circ C$	Power Dissipation	40	W
	Linear Derating Factor	0.32	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
E_{AS}	Single Pulse Avalanche Energy ②	290	mJ
I_{AR}	Avalanche Current ③	9.9	A
E_{AR}	Repetitive Avalanche Energy ④	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.27	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	—	—	0.18	Ω	$V_{GS} = 5.0V, I_D = 5.9A$ ④
		—	—	0.27		$V_{GS} = 4.0V, I_D = 5.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	16	—	—	S	$V_{DS} = 50V, I_D = 10A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V, V_{GS} = 0V, T_J = 160^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -10V$
Q_g	Total Gate Charge	—	—	66	nA	$I_D = 17A$ $V_{DS} = 160V$ $V_{GS} = 10V$, See Fig. 6 and 13 ④
Q_{gs}	Gate-to-Source Charge	—	—	9.0		
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	38		
$t_{d(on)}$	Turn-On Delay Time	—	8.0	—		
t_r	Rise Time	—	83	—	ns	$V_{DD} = 100V$ $I_D = 17A$ $R_G = 4.6\Omega$ $R_D = 5.7\Omega$, See Fig. 10 ④
$t_{d(off)}$	Turn-Off Delay Time	—	44	—		
t_f	Fall Time	—	52	—		
L_D	Internal Drain Inductance	—	4.5	—		
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
C_{iss}	Input Capacitance	—	1800	—		
C_{oss}	Output Capacitance	—	400	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz$, See Fig. 5
C_{rss}	Reverse Transfer Capacitance	—	120	—		


Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	9.9	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	40		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	$T_J = 25^\circ\text{C}, I_S = 9.9A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	310	470	ns	$T_J = 25^\circ\text{C}, I_F = 17A$
Q_{rr}	Reverse Recovery Charge	—	3.2	4.8	μC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

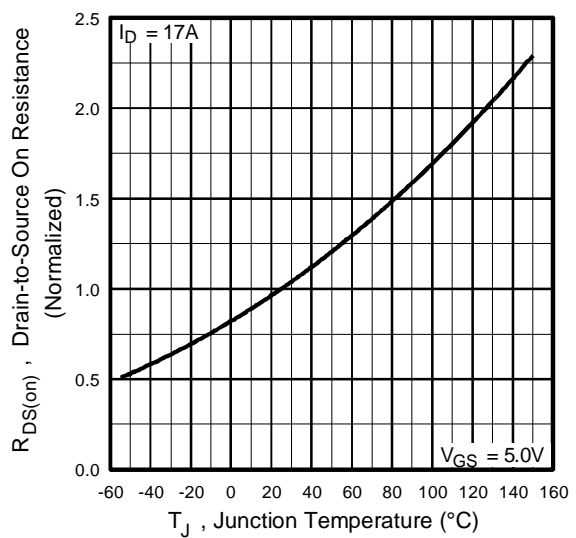
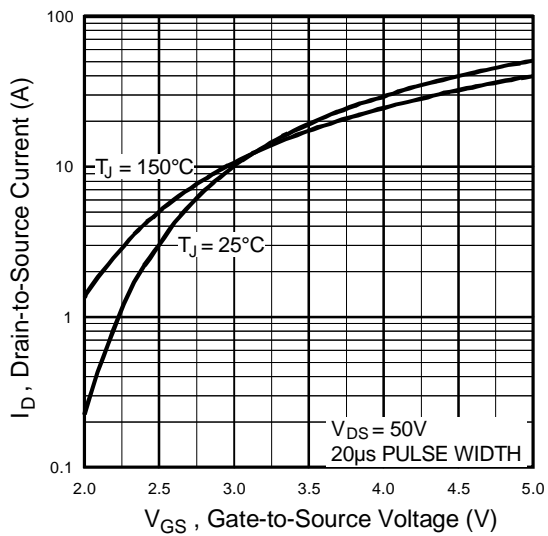
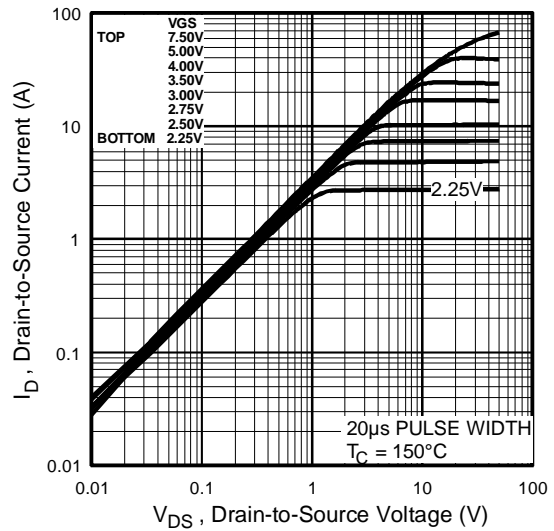
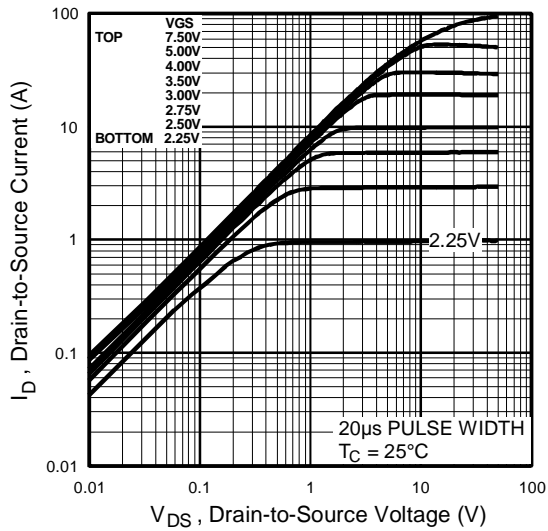
① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② $I_{SD} \leq 17A, di/dt \leq 150A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$

③ $t=60s, f=60Hz$

④ $V_{DD} = 25V$, starting $T_J = 25^\circ\text{C}$, $L = 4.4mH$
 $R_G = 25\Omega, I_{AS} = 9.9A$. (See Figure 12)

⑤ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.



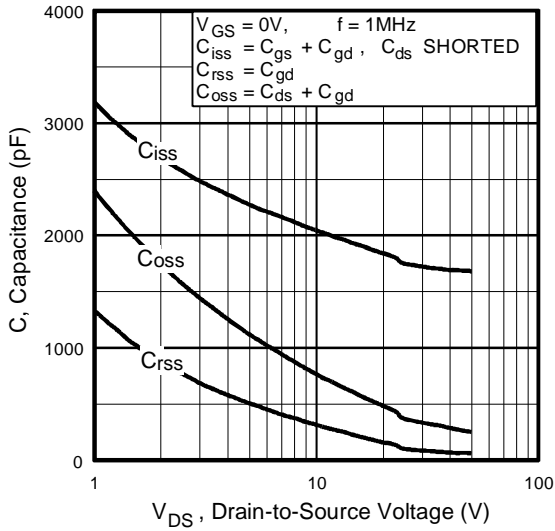


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

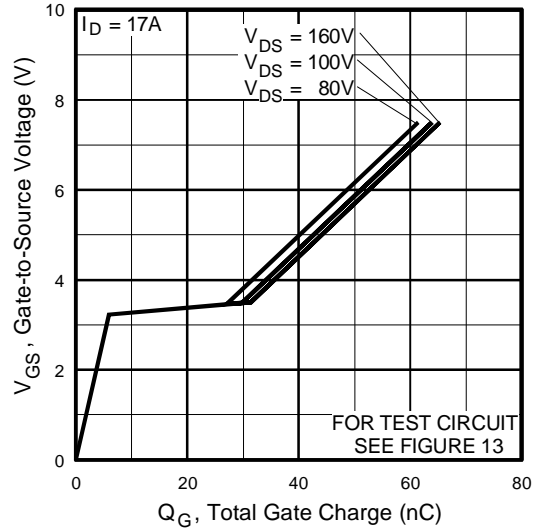


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

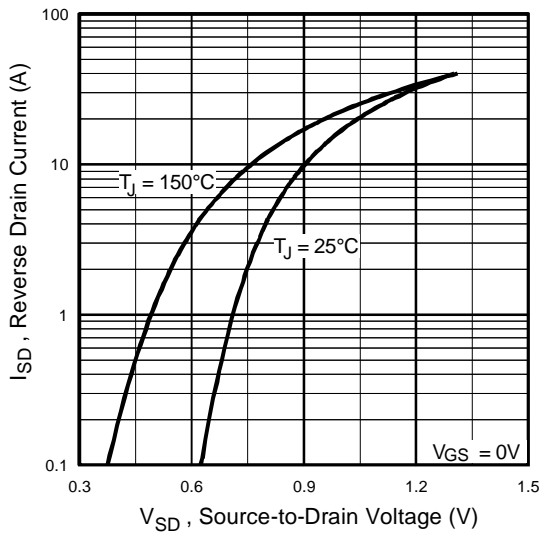


Fig 7. Typical Source-Drain Diode Forward Voltage

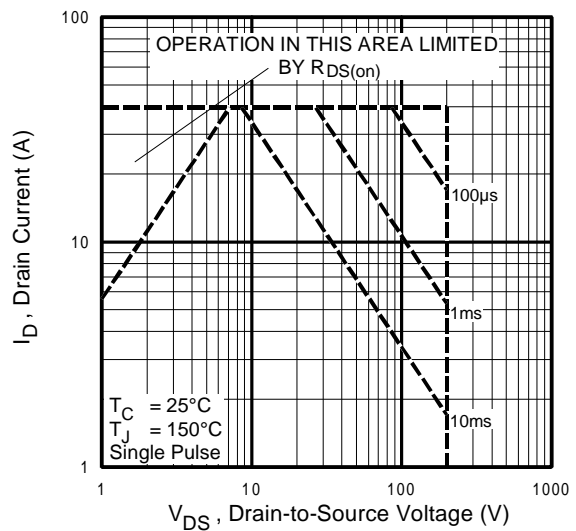


Fig 8. Maximum Safe Operating Area

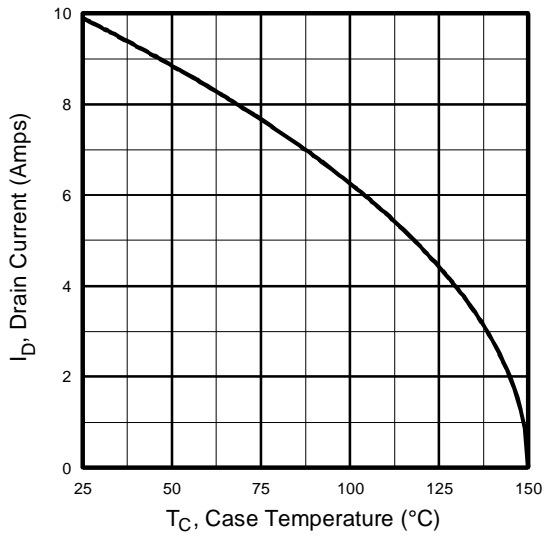


Fig 9. Maximum Drain Current Vs. Case Temperature

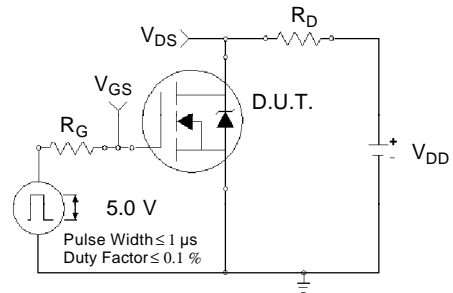


Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

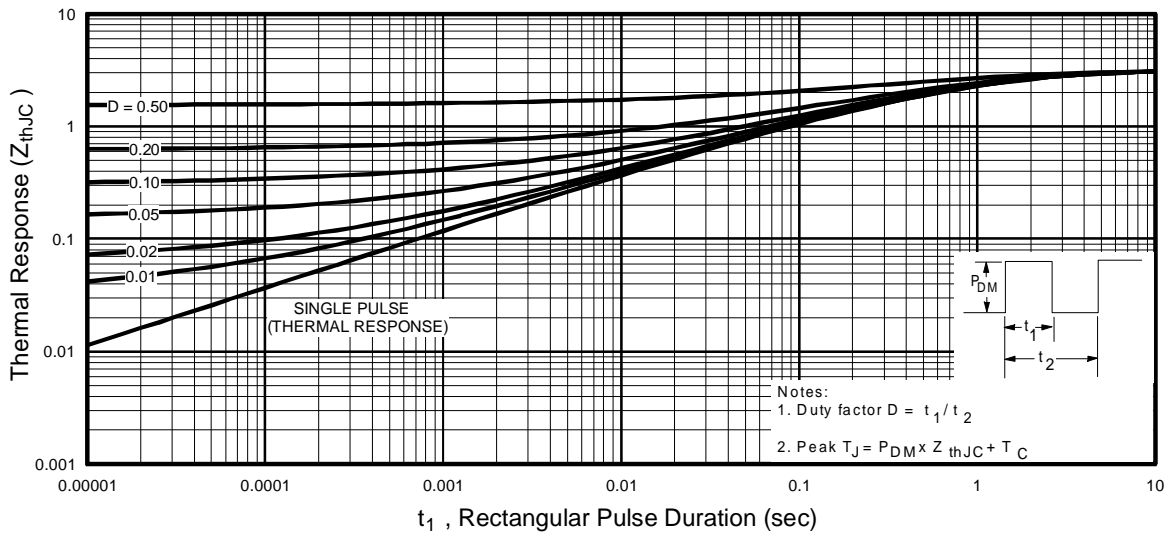


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

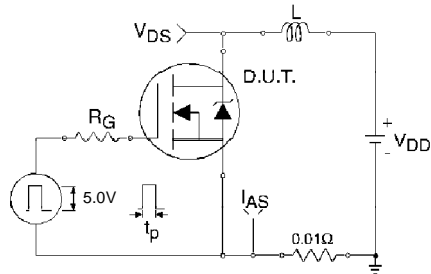


Fig 12a. Unclamped Inductive Test Circuit

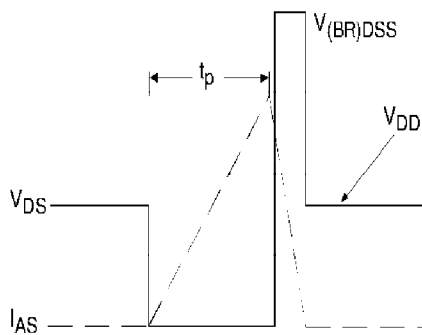


Fig 12b. Unclamped Inductive Waveforms

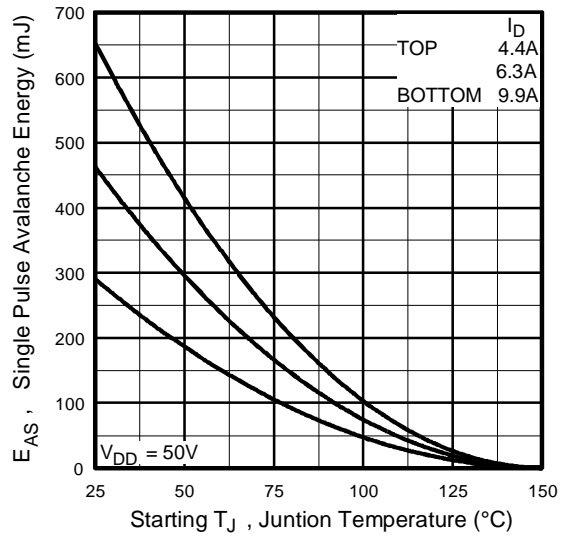


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

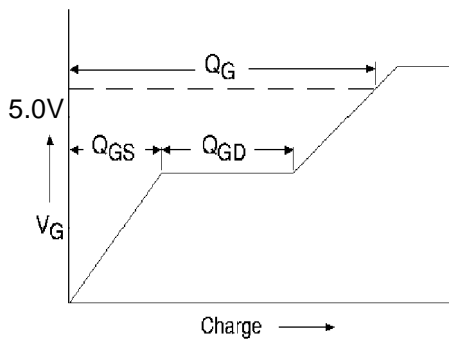


Fig 13a. Basic Gate Charge Waveform

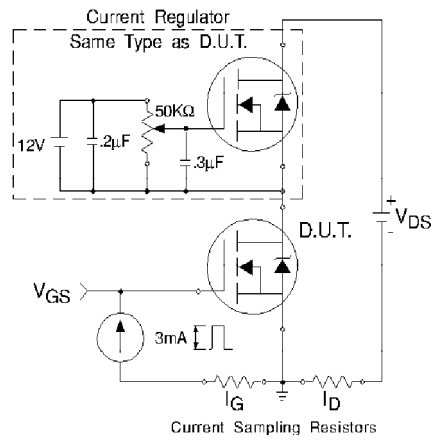
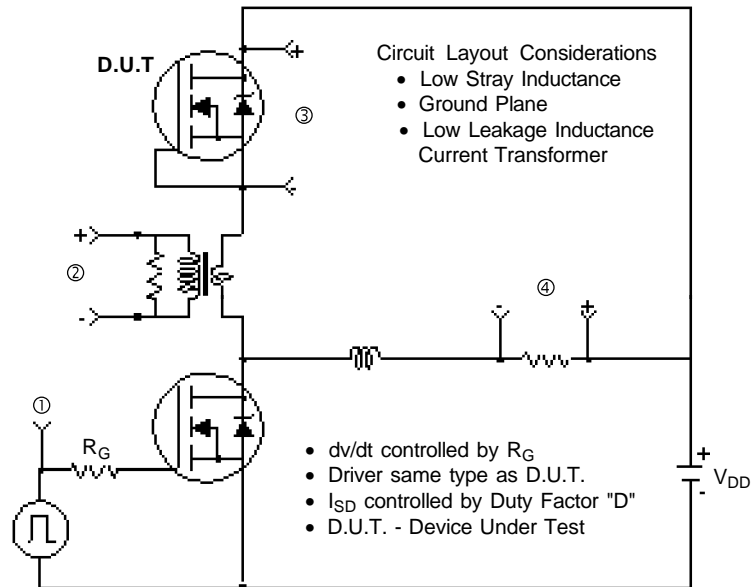


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



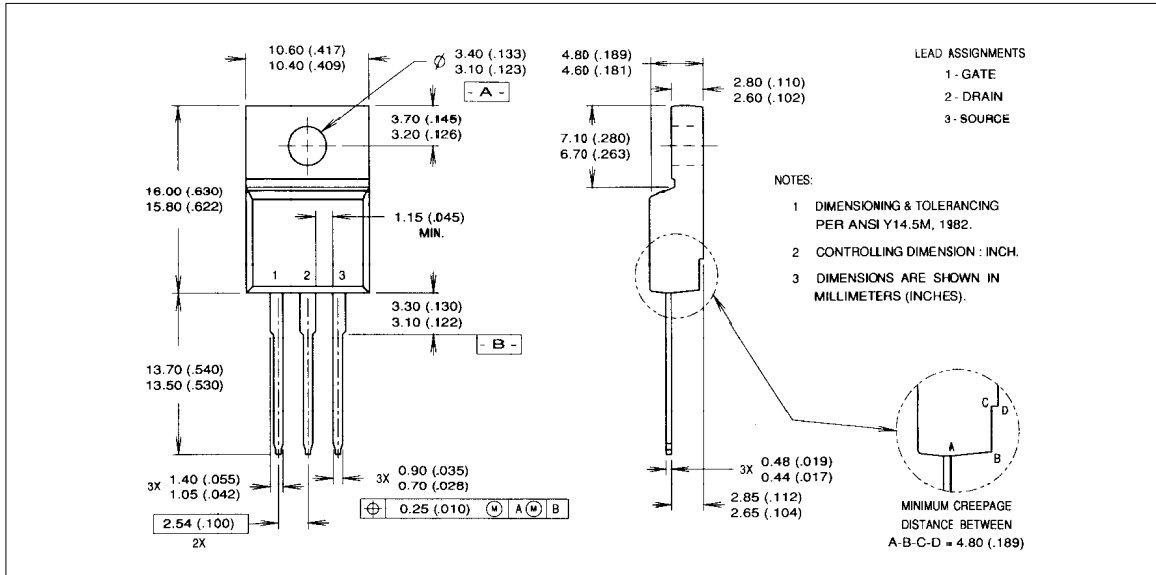
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

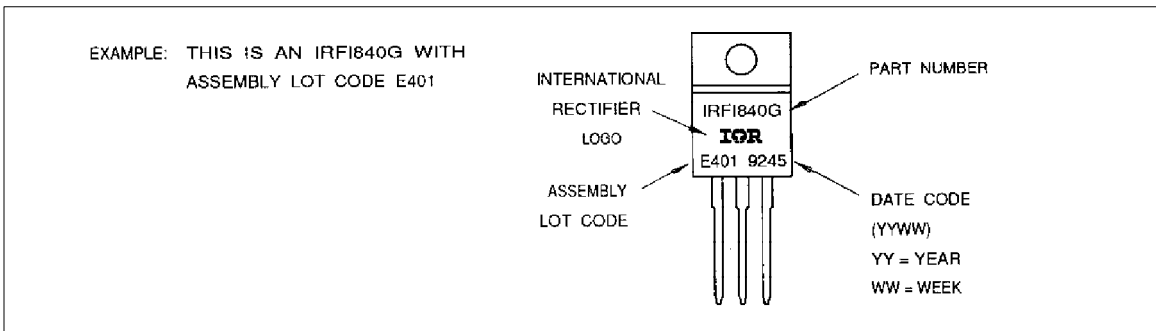
IRLI640G



Package Outline TO-220 Full-Pak



Part Marking Information TO-220 Full-Pak



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Data and specifications subject to change without notice.