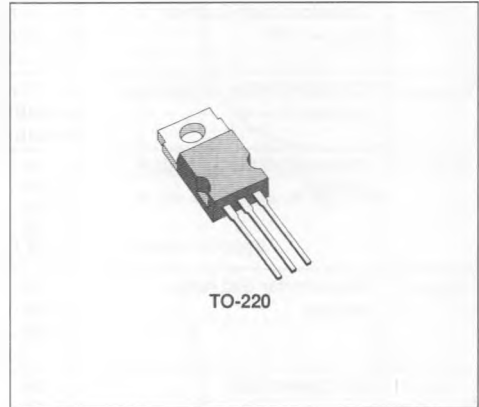


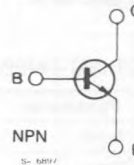
## MOTOR CONTROL, SWITCH REGULATORS

### DESCRIPTION

The MJE13006, MJE13007 and MJE13007A are silicon multiepitaxial mesa NPN transistors. They are mounted in Jedec TO-220 plastic package, intended for use in motor controls, switching regulator's etc.



### INTERNAL SCHEMATIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		MJE13006	MJE13007	MJE13007A	
$V_{CE0}$	Collector-emitter Voltage ( $V_B = 0$ )	300	400	400	V
$V_{CEV}$	Collector-emitter Voltage	600	700	850	V
$V_{EBO}$	Emitter-base Voltage ( $I_C = 0$ )	9			V
$I_C$	Collector Current	8			A
$I_{CM}$	Collector Peak Current	16			A
$I_B$	Base Current	4			A
$I_{BM}$	Base Peak Current	8			A
$I_E$	Emitter Current	12			A
$I_{EM}$	Emitter Peak Current	24			A
$P_{Tot}$	Total Power Dissipation at $T_{case} \leq 25^\circ C$	80			W
$T_{stg}$	Storage Temperature	- 65 to 150			$^\circ C$
$T_J$	Junction Temperature	150			$^\circ C$

**THERMAL DATA**

$R_{th(j-case)}$	Thermal Resistance Junction-case	Max	1.56	°C/W
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**ELECTRICAL CHARACTERISTICS** ( $T_{case} = 25^{\circ}C$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	
$I_{EBO}$	Emitter Cutoff Current ( $I_C = 0$ )	$V_{EB} = 9V$			1	mA	
$I_{CEV}$	Collector Cutoff Current ( $V_{BE} = 1.5V$ )	$V_{CEV} = \text{rated value}$ $V_{CEV} = \text{rated value}$ $T_{case} = 100^{\circ}C$			1	mA	
					5	mA	
$V_{CEO(sus)}^*$	Collector-Emitter Sustaining Voltage ( $I_B = 0$ )	$I_C = 10\text{ mA}$ for <b>MJE13006</b> for <b>MJE13007/13007A</b>	300 400			V V	
$V_{CE(sat)}^*$	Collector-emitter Saturation Voltage	$I_C = 2A$ $I_B = 0.4A$			1	V	
		$I_C = 5A$ $I_B = 1A$			1.5	V	
		$I_C = 8A$ $I_B = 2A$			3	V	
		$I_C = 5A$ $I_B = 1A$ $T_{case} = 100^{\circ}C$			2	V	
$V_{BE(sat)}^*$	Base-emitter Saturation Voltage	$I_C = 2A$ $I_B = 0.4A$			1.2	V	
		$I_C = 5A$ $I_B = 1A$			1.6	V	
		$I_C = 5A$ $I_B = 1A$					
		$T_{case} = 100^{\circ}C$			1.5	V	
$h_{FE}^*$	DC Current Gain	$I_C = 2A$ $V_{CE} = 5V$	8		40		
		$I_C = 5A$ $V_{CE} = 5V$	6		30		
$f_T$	Transition Frequency	$I_C = 500\text{mA}$ $V_{CE} = 10V$ $f = 1\text{MHz}$	4			MHz	
$C_{CBO}$	Output Capacitance	$V_{CB} = 10V$ $I_E = 0$ $f = 0.1\text{MHz}$		110		pF	

**RESISTIVE SWITCHING TIMES** (fig. 2)

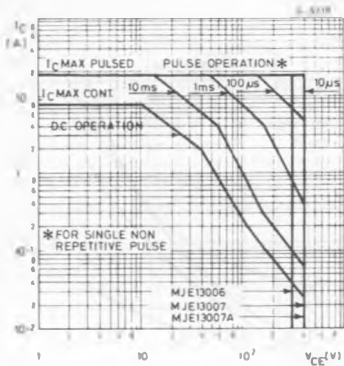
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{on}$	Turn-on Time	$V_{CC} = 125V$ $I_C = 5A$ $I_{B1} = -I_{B2} = 1A$ $t_p = 25\mu s$ Duty Cycle < 1%			0.7	$\mu s$
$t_s$	Storage Time				3	$\mu s$
$t_f$	Fall Time				0.7	$\mu s$

**INDUCTIVE SWITCHING TIMES** (fig. 1)

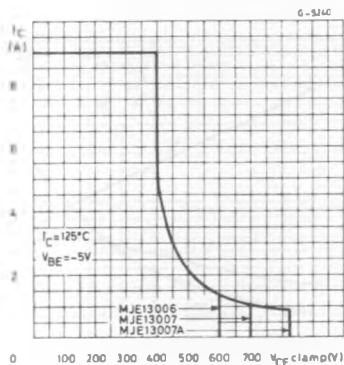
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_f$	Fall Time	$V_{CC} = 125V$ $I_C = 5A$ $I_{B1} = 1A$ $t_p = 25\mu s$ Duty Cycle < 1% $T_{case} = 100^{\circ}C$			0.3	$\mu s$
		$V_{CC} = 125V$ $I_C = 5A$ $I_{B1} = 1A$ $t_p = 25\mu s$ Duty Cycle $\leq 1\%$			0.6	$\mu s$

\* Pulsed : pulse duration  $\leq 300 \mu s$ , duty cycle < 1.5 %.

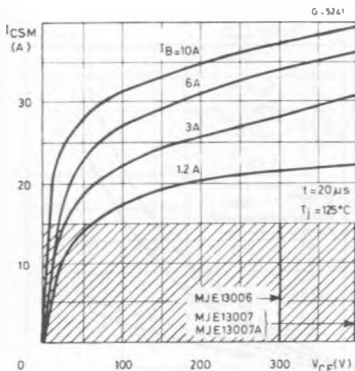
Safe Operating Areas.



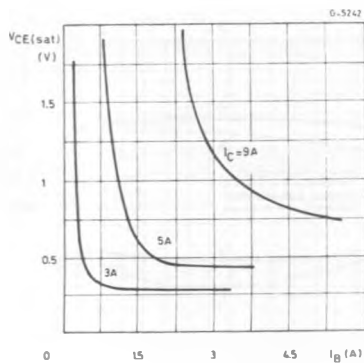
Clamped Reverse Bias operating Areas.



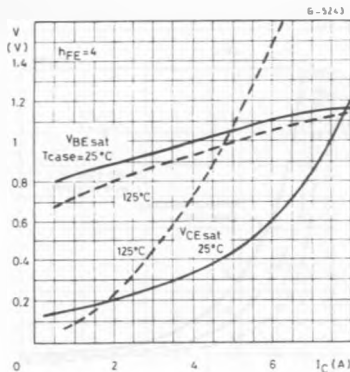
Forward Biased Accidental Overload Area (see fig. 3).



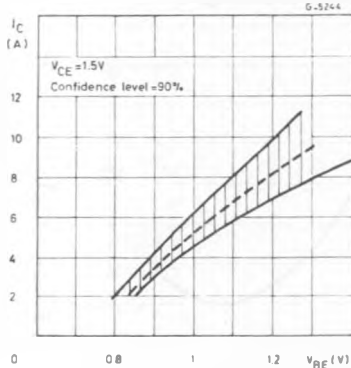
Collector Saturation Voltage.



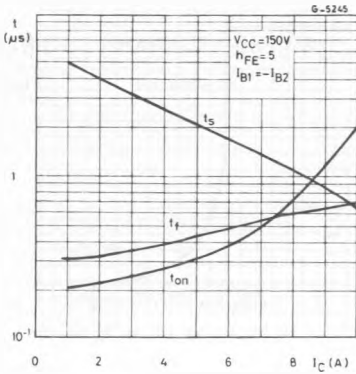
Saturation Voltages.



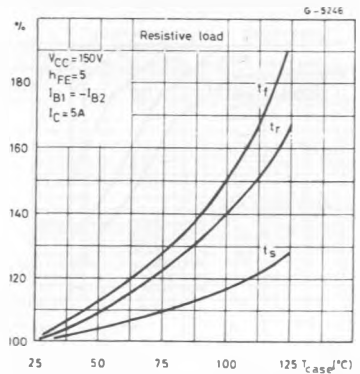
Collector Current Spread vs. Emitter Voltage.



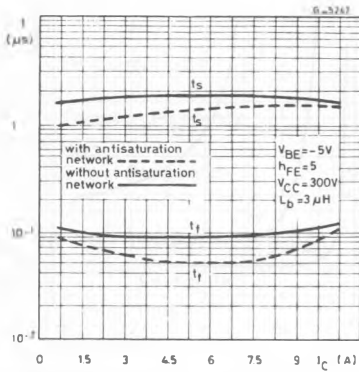
Switching Times Resistive Load (see fig. 2).



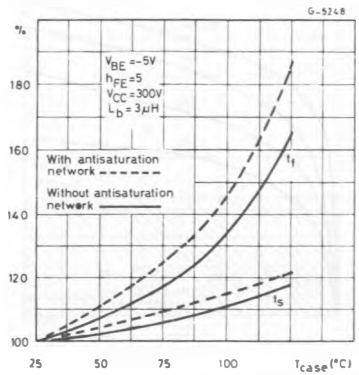
Switching Times Percentage Variation vs. Case Temperature.



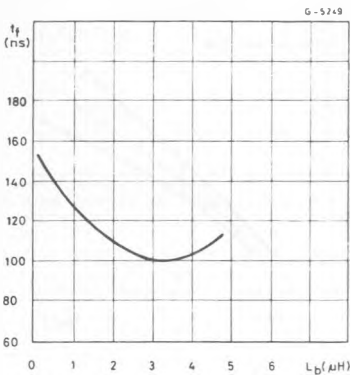
Switching Times Inductive Load (see fig. 1).



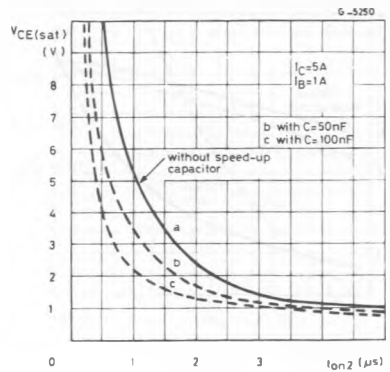
Switching Times Inductive Load vs. Case Temperature.



Fall Times vs. Lb (see fig. 1).



Dynamic Collector-emitter Saturation Voltage (see fig. 4).



DC Current Gain.

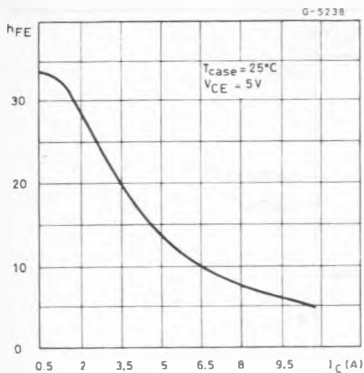


Figure 1 : Switching Times Test Circuit on Inductive Load, with and without Antisaturation Network.

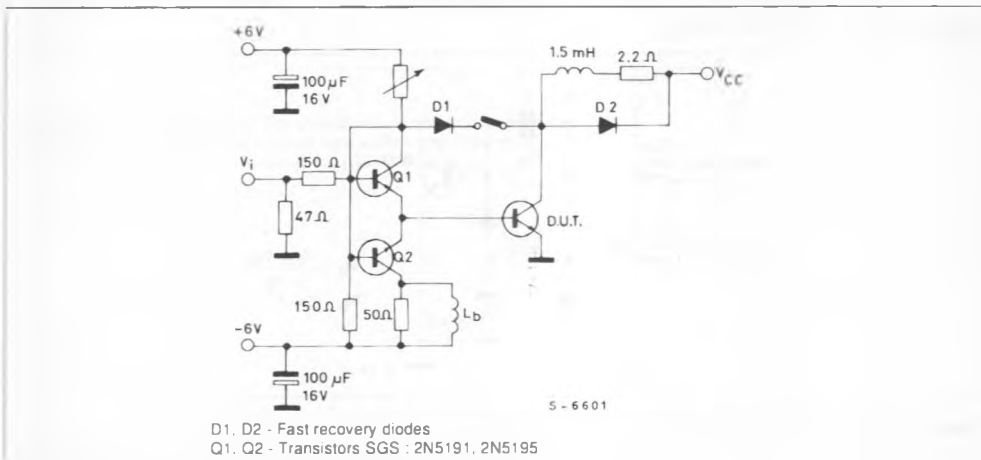


Figure 2 : Switching Times Test Circuit on Resistive Load.

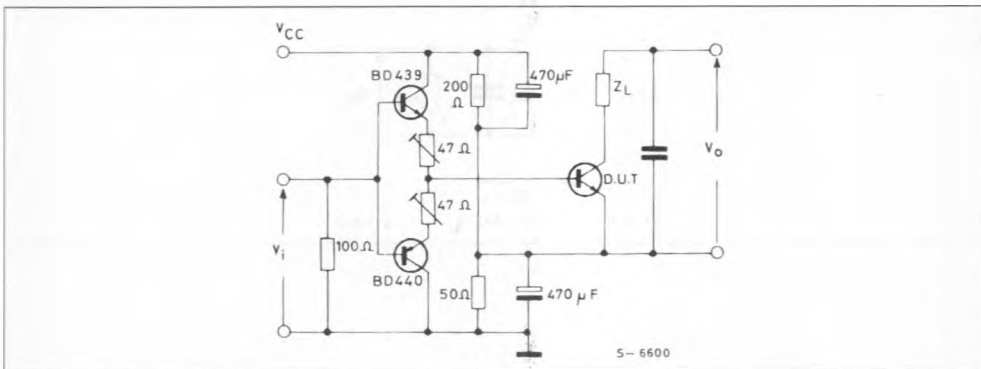


Figure 3 : Forward Biased Accidental Overload Area Test Circuit.

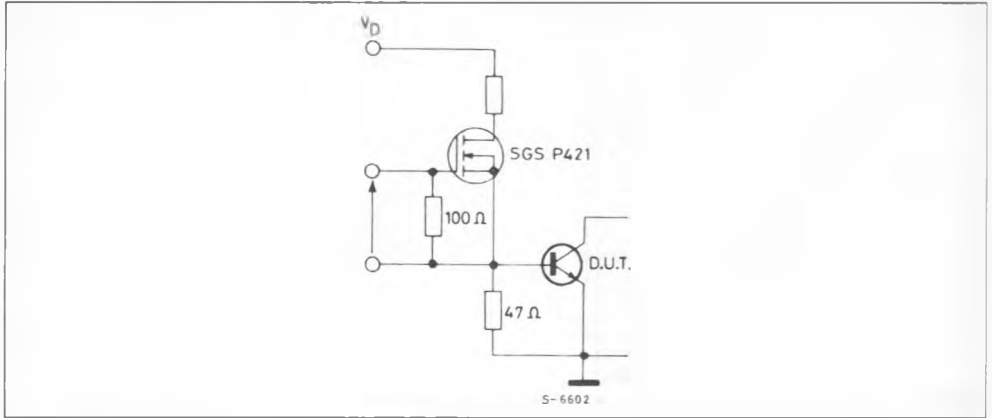


Figure 4 :  $V_{CE(sat)}$  Dyn. Test Circuit.

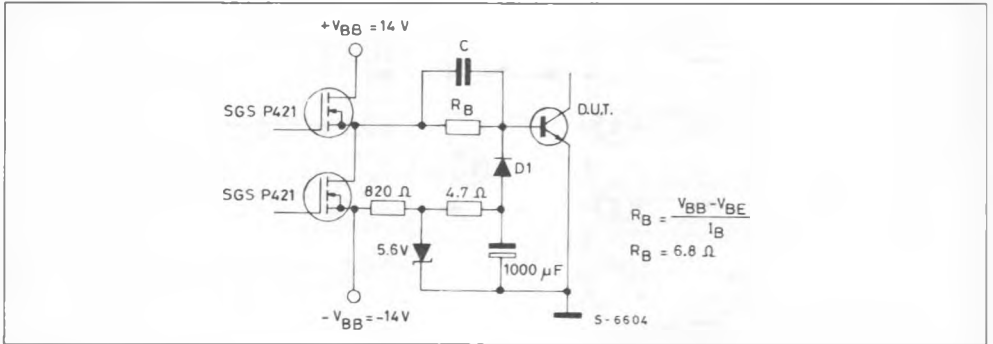


Figure 5 : Equivalent Input Schematic Circuit at Turn-on.

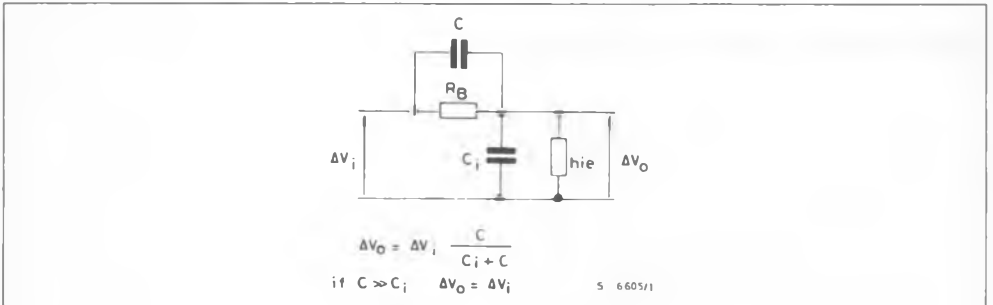
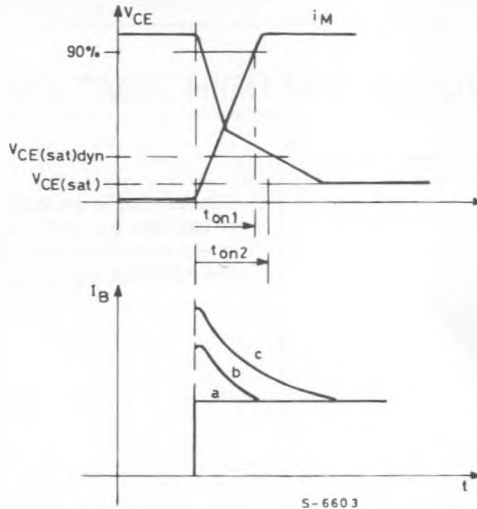


Figure 6 : Remarks to  $V_{CE(sat)}$  Dyn. Test Circuit (fig. 4).



The speed-up capacitor decreases the  $V_{CE(sat)}$  dyn. as shown in diagram (figure 6).  
 The 50 nF capacitor modifies the shape of base current with a overshoot