SGS-THOMSON MICROELECTRONICS

MTH6N60FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

PRELIMINARY DATA

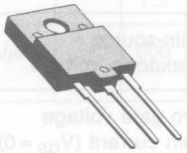
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
MTH6N60FI	600 V	1.2 Ω	3.5 A

- HIGH VOLTAGE - 600 V FOR OFF-LINE APPLICATIONS
- ULTRA FAST SWITCHING TIMES FOR OPERATIONS AT > 100KHz
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

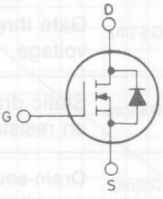
- SWITCHING POWER SUPPLY
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make these POWER MOS ideal for very high speed switching applications. Typical uses include SMPS, uninterruptible power supplies and motor controls.



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	600	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	600	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c = 25°C$	3.5	A
I_{DM}	Drain current (pulsed)	14	A
P_{tot}	Total dissipation at $T_c < 25°C$	40	W
	Derating factor	0.32	W/°C
T_{stg}	Storage temperature	– 65 to 150	°C
T_j	Max. operating junction temperature	150	°C

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	3.12	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient		62.5	°C/W

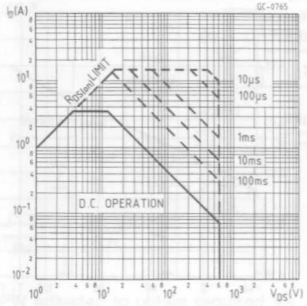
ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8	T_c = 125°C			200 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±500	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA V_{DS} = V_{GS} I_D = 1 mA	 T_c = 100°C	2 1.5		4.5 4	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 3 A				1.2	Ω
$V_{DS(on)}$	Drain-source on voltage	V_{GS} = 10 V I_D = 6 A V_{GS} = 10 V I_D = 3 A	 T_c = 100°C			8 7.2	V V
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 10 V	I_D = 3 A	2			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			1800 350 150	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V R_i = 50 Ω	I_D = 3 A V_i = 10 V			60 150 200 120	ns ns ns ns

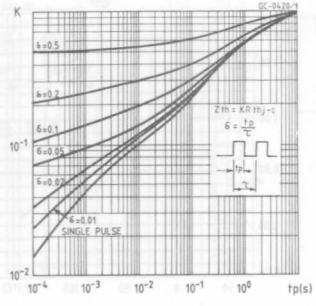
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)					3.5 14	A A
V_{SD}	Forward on voltage	I_{SD} = 6 A	V_{GS} = 0		1.3		V
t_{rr}	Reverse recovery time	I_{SD} = 6 A	di/dt = 100A/μs		600		ns

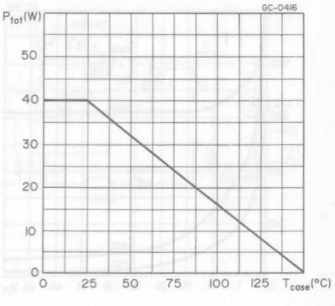
Safe operating areas



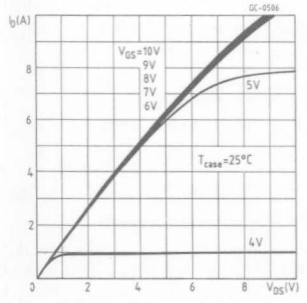
Thermal impedance



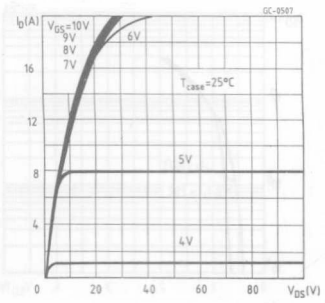
Derating curve



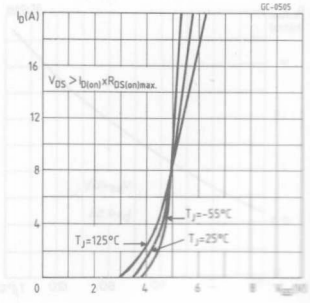
Output characteristics



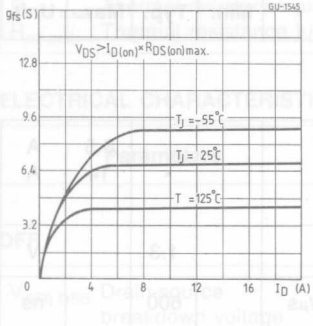
Output characteristics



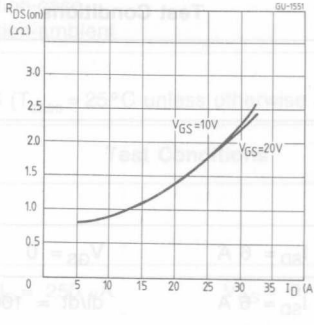
Transfer characteristics



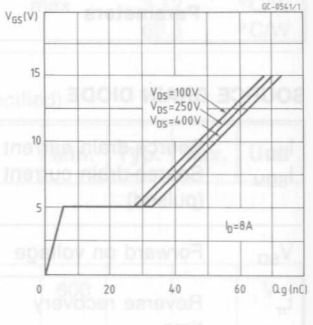
Transconductance



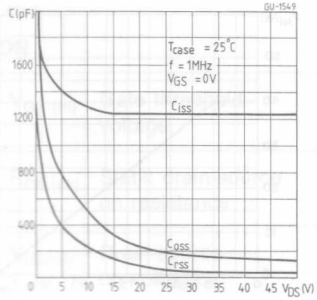
Static drain-source on resistance



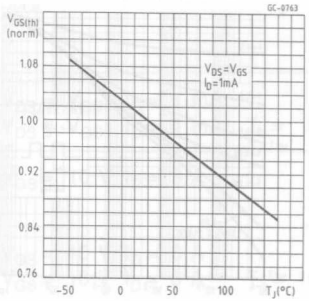
Gate charge vs gate-source voltage



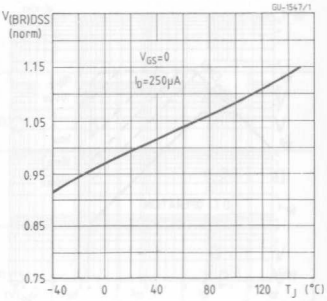
Capacitance variation



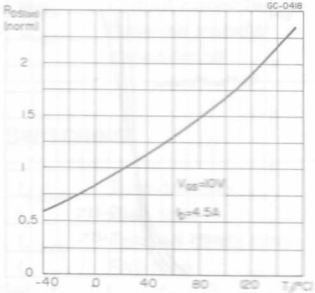
Normalized gate threshold voltage vs temperature



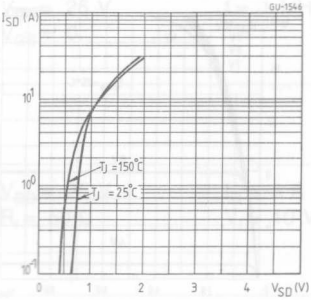
Normalized breakdown voltage vs temperature



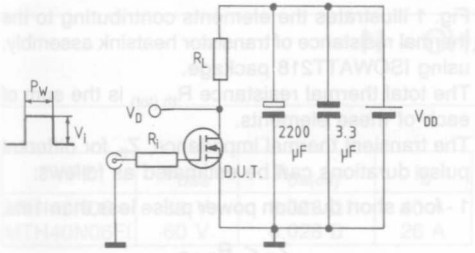
Normalized on resistance vs temperature



Source-drain diode forward characteristics

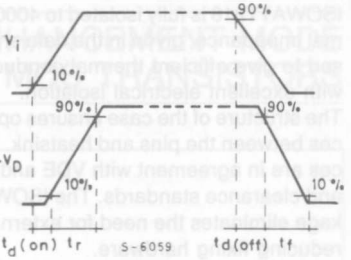


Switching times test circuit for resistive load

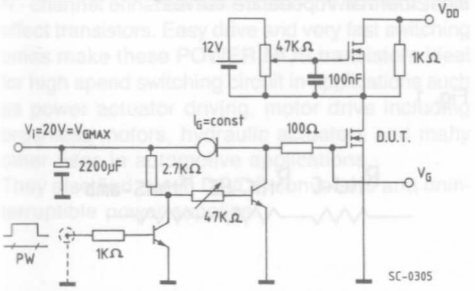


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

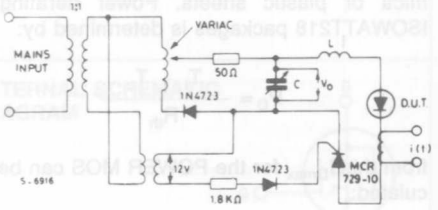


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



ISOWATT218 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT218 is fully isolated to 4000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. These distances are in agreement with VDE and UL creepage and clearance standards. The ISOWATT218 package eliminates the need for external isolation so reducing fixing hardware.
The package is supplied with leads longer than the standard TO-218 to allow easy mounting on pcbs.
Accurate moulding techniques used in manufacture assures consistent heat spreader-to-heatsink capacitance
ISOWATT218 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT218 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT218 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT218 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1