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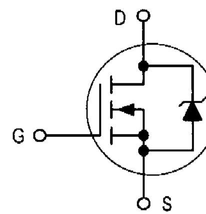
MTP2N60E

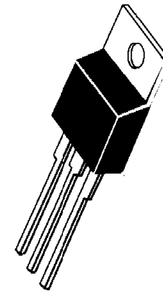
TMOS E-FET ™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

TMOS POWER FET
2.0 AMPERES
600 VOLTS
$R_{DS(on)}$ = 3.8 OHMS

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature

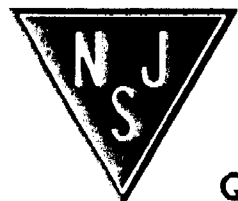




TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	600	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–to–Source Voltage — Continuous — Single Pulse ($t_p \le 50$ μs)	V_{GS}	±20 ±40	Vdc
Drain Current — Continuous — Single Pulse ($t_p \le 10$ μs)	I_D I_{DM}	2.0 9.0	Adc
Total Power Dissipation Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10 Vdc, L = 95 mH, R_G = 25 Ω, Peak I_L = 2.0 Adc)	E_{AS}	190	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C



NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However, NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.

Quality Semi-Conductors

MTP2N60E

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (positive)		$V_{(BR)DSS}$	600 —	— 480	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 480 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	0.25 1.0	mA
Gate–Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0 Vdc)		I_{GSSF}	—	—	100	nAdc
Gate–Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0 Vdc)		I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (negative)		$V_{GS(th)}$	2.0 —	3.1 8.5	4.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	—	3.3	3.8	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2.0 Adc) (V_{GS} = 10 Vdc, I_D = 1.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	— —	8.2 8.4	Vdc
Forward Transconductance (V_{DS} ≥ 50 Vdc, I_D = 1.0 Adc)		g_{FS}	1.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	435	—	pF
Reverse Transfer Capacitance		C_{rss}	—	56	—	
Output Capacitance		C_{oss}	—	9.2	—	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 300 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_g = 18 Ω)	$t_{d(on)}$	—	12	—	ns
Rise Time		t_r	—	21	—	
Turn–Off Delay Time		$t_{d(off)}$	—	30	—	
Fall Time		t_f	—	24	—	
Gate Charge	(V_{DS} = 400 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	13	22	nC
		Q_1	—	2.0		
		Q_2	—	6.0	—	
		Q_3	—	5.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.6	Vdc
	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.9	—	
Reverse Recovery Time	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	340	—	ns
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain 0.25″ from package to center of die)		L_d	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source pin 0.25″ from package to source bond pad.)		L_s	—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) Switching characteristics are independent of operating junction temperature.