

**S G S-THOMSON N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS**

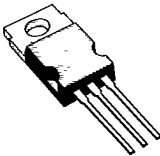
TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub> -	I <sub>D</sub> ■
MTP3055A	60 V	0.15 Ω	12 A
MTP3055AFI	60 V	0.15 Ω	10 A

- ULTRA FAST SWITCHING - UP TO > 100KHz
- LOW DRIVE ENERGY FOR EASY DRIVE REDUCES SIZE AND COST
- INTEGRAL SOURCE - DRAIN DIODE

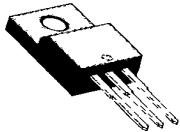
**INDUSTRIAL APPLICATIONS:**

- GENERAL PURPOSE SWITCH
- SERIES REGULATOR

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast times make these POWER MOS transistors ideal for high speed switching circuit in applications such as power actuator driving, motor drive including brushless motors, robotics, actuators lamp driving, series regulator and many other uses in industrial control applications. They also find use in DC/DC converters and uninterruptible power supplies.



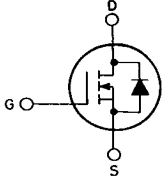
**TO-220**



**ISOWATT220**

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**INTERNAL SCHEMATIC DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

	TO-220 ISOWATT220		MTP3055A MTP3055AFI	
	V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)		60
V <sub>DGR</sub>	Drain-gate voltage (R <sub>GS</sub> = 20 KΩ)		60	V
V <sub>GS</sub>	Gate-source voltage		±20	V
I <sub>DM</sub>	Drain current (pulsed)		26	A
I <sub>GM</sub>	Gate current (pulsed)		1.5	A
I <sub>D</sub> ■	Drain current (continuous)		<b>TO-220</b> 12	<b>ISOWATT220</b> 10 A
P <sub>tot</sub> ■	Total dissipation at T <sub>c</sub> < 25°C		40	30 W
■	Derating factor		0.32	0.24 W/°C
T <sub>stg</sub>	Storage temperature		-65 to 150 °C	
T <sub>j</sub>	Max. operating junction temperature		150 °C	

■ See note on ISOWATT220 in this datasheet

## THERMAL DATA ■

TO-220

ISOWATT220

$R_{th(j-c)}$	Thermal resistance junction-case	max	3.12	4.16	°C/W
$T_I$	Maximum lead temperature for soldering purpose	max	275		°C

ELECTRICAL CHARACTERISTICS ( $T_{case} = 25^\circ\text{C}$  unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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## OFF

$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ $V_{GS} = 0$	60		V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_c = 125^\circ\text{C}$		50 1000	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 \text{ V}$		$\pm 100$	nA

## ON \*

$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 1 \text{ mA}$ $V_{DS} = V_{GS}$ $I_D = 1 \text{ mA}$ $T_c = 100^\circ\text{C}$	2 1.5		4.5 4	V V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ $I_D = 6 \text{ A}$		0.15	$\Omega$	
$V_{DS(on)}$	Drain-source on voltage	$V_{GS} = 10 \text{ V}$ $I_D = 12 \text{ A}$ $V_{GS} = 10 \text{ V}$ $I_D = 6 \text{ A}$ $V_{GS} = 10 \text{ V}$ $I_D = 6 \text{ A}$ $T_c = 100^\circ\text{C}$			2.0 0.9 1.5	V V V

## DYNAMIC

$g_{fs}^*$	Forward transconductance	$V_{DS} = 10 \text{ V}$ $I_D = 6 \text{ A}$	4.5			mho
$C_{iss}$	Input capacitance	$V_{DS} = 25 \text{ V}$ $f = 1 \text{ MHz}$ $V_{GS} = 0$			500	pF
$C_{oss}$	Output capacitance				200	pF
$C_{rss}$	Reverse transfer capacitance				100	pF
$Q_g$	Total gate charge	$V_{DS} = 48 \text{ V}$ $I_D = 12 \text{ A}$ $V_{GS} = 10 \text{ V}$			17	nC

## SWITCHING

$t_{d(on)}$	Turn-on time	$V_{DD} = 25 \text{ V}$ $I_D = 6 \text{ A}$ $R_{gen} = 50 \Omega$			20	ns
$t_r$	Rise time				60	ns
$t_{d(off)}$	Turn-off delay time				65	ns
$t_f$	Fall time				65	ns

ELECTRICAL CHARACTERISTICS (Continued)

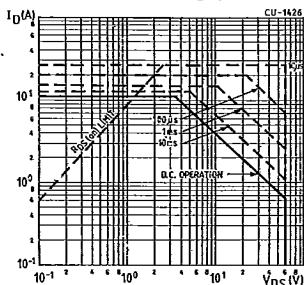
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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SOURCE DRAIN DIODE

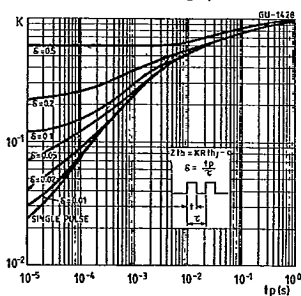
$V_{SD}$	Forward on voltage	$I_{SD} = 12\text{ A}$	$V_{GS} = 0$	2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 12\text{ A}$	$V_{GS} = 0$	75	ns

- \* Pulsed: Pulse duration  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$
- See note on ISOWATT220 in this datasheet

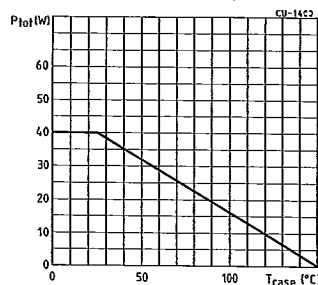
Safe operating areas (standard package)



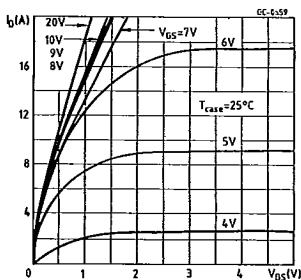
Thermal impedance (standard package)



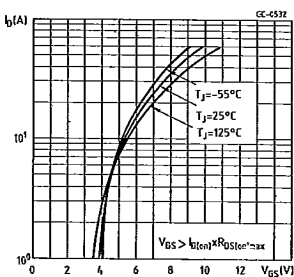
Derating curve (standard package)



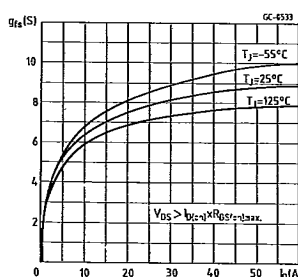
Output characteristics



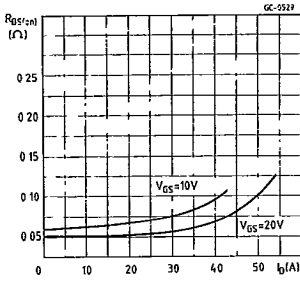
Transfer characteristics



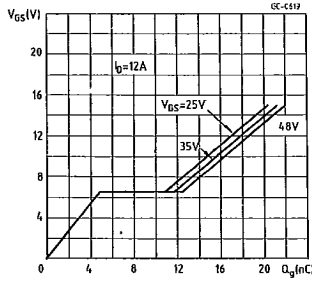
Transconductance



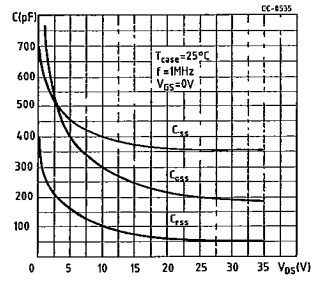
Static drain-source on resistance



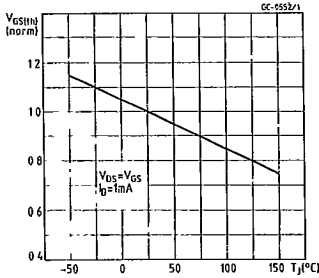
Gate charge vs gate-source voltage



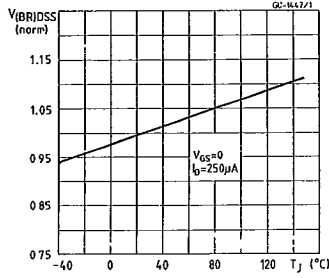
Capacitance variation



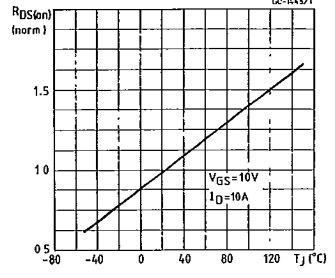
Normalized gate threshold voltage vs temperature



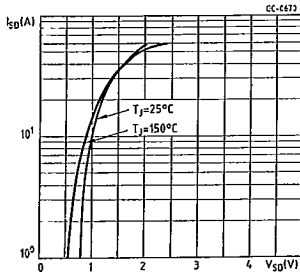
Normalized breakdown voltage vs temperature



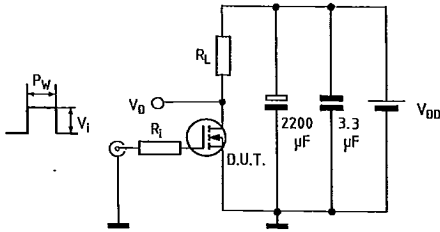
Normalized on resistance vs temperature



Source-drain diode forward characteristics



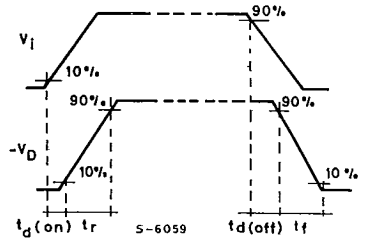
Switching times test circuit for resistive load



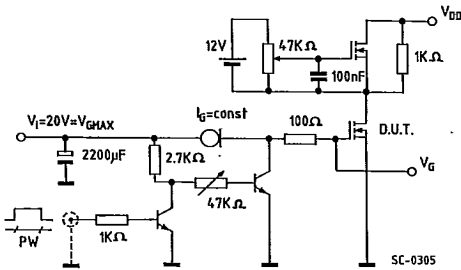
Pulse width  $\leq 100 \mu\text{s}$   
Duty cycle  $\leq 2\%$

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Switching time wavetforms for resistive load

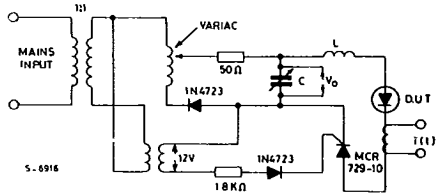


Gate charge test circuit



PW adjusted to obtain required  $V_G$

Body-drain diode  $t_{rr}$  measurement  
Jedec test circuit



**ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.**

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimized to give efficient thermal conduction together with excellent electrical isolation.

The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.

ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_J - T_C}{R_{th}}$$

from this  $I_{Dmax}$  for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)} \text{ (at } 150^\circ\text{C)}}}$$

**THERMAL IMPEDANCE OF ISOWATT220 PACKAGE**

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.

The total thermal resistance  $R_{th(tot)}$  is the sum of each of these elements.

The transient thermal impedance,  $Z_{th}$  for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ-C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

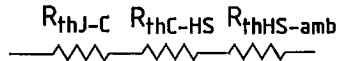
$$Z_{th} = R_{thJ-C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ-C} + R_{thC-HS} + R_{thHS-amb}$$

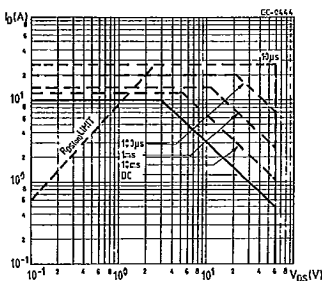
It is often possible to discern these areas on transient thermal impedance curves.

Fig. 1

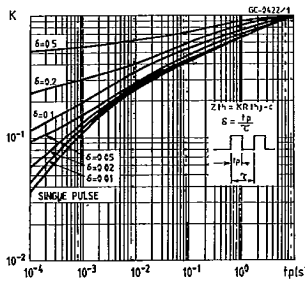


**ISOWATT DATA**

**Safe operating areas**



**Thermal impedance**



**Derating curve**

