

Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

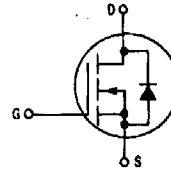
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTM3N60
MTP3N55
MTP3N60

TMOS POWER FETs
 3 AMPERES
 $I_{DS(on)} = 2.5$ OHMS
 550 and 600 VOLTS



MAXIMUM RATINGS

Rating	Symbol	MTP3N55	MTM3N60 MTP3N60	Unit
Drain-Source Voltage	V_{DS}	550	600	Vdc
Drain-Gate Voltage ($R_{GS} = 1$ MΩ)	V_{DGR}	550	600	Vdc
Gate-Source Voltage — Continuous	V_{GS}		±20	Vdc
— Non-repetitive ($t_p \leq 50 \mu s$)	V_{GSM}		±40	Vpk
Drain Current Continuous	I_D	3		Adc
Pulsed	I_{DM}	10		
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	75	0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	1.67	
Junction to Ambient	$R_{\theta JA}$	30	
		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

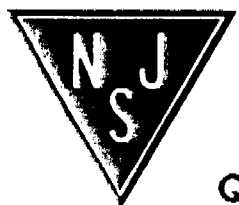


MTM3N60
 TO-204AA



MTP3N55
 MTP3N60
 TO-220AB

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($V_{GS} = 0, I_D = 0.25 \text{ mA}$)	MTP3N55 MTM/MTP3N60	$V_{(BR)DSS}$	550 600	— —	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0$) ($V_{DS} = 0.8 \text{ Rated } V_{DSS}, V_{GS} = 0, T_J = 125^\circ\text{C}$)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward ($V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0$)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0$)		I_{GSSR}	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1 \text{ mA}$) $T_J = 100^\circ\text{C}$		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10 \text{ Vdc}, I_D = 1.5 \text{ Adc}$)		$r_{DS(on)}$	—	2.5	Ohms
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_D = 3 \text{ Adc}$) ($I_D = 1.5 \text{ Adc}, T_J = 100^\circ\text{C}$)		$V_{DS(on)}$	— —	9 7.5	Vdc
Forward Transconductance ($V_{DS} = 15 \text{ V}, I_D = 1.5 \text{ A}$)		g_{FS}	1.5	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 26 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz})$ See Figure 11	C_{iss}	—	1000	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{ras}	—	80	

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	$(V_{DD} = 25 \text{ V}, I_D = 0.5 \text{ Rated } I_D,$ $R_{gen} = 50 \text{ ohms})$ See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	100	
Turn-Off Delay Time		$t_{d(off)}$	—	180	
Fall Time		t_f	—	80	
Total Gate Charge	$(V_{DS} = 0.8 \text{ Rated } V_{DSS},$ $I_D = \text{Rated } I_D, V_{GS} = 10 \text{ V})$ See Figure 12	Q_g	16 (Typ)	18	nC
Gate-Source Charge		Q_{gs}	8 (Typ)	—	
Gate-Drain Charge		Q_{gd}	8 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	$(I_S = \text{Rated } I_D,$ $V_{GS} = 0)$	V_{SD}	1.1 (Typ)	—	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	165 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE (TO-204)

Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)	L_s	12.5 (Typ)	—	nH

INTERNAL PACKAGE INDUCTANCE (TO-220)

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	7.5 (Typ)	—	nH

*Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

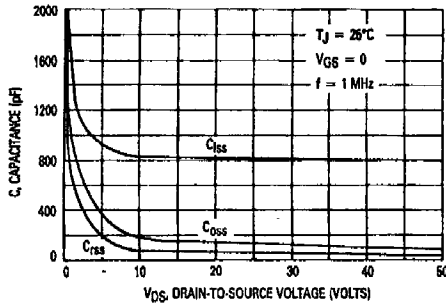


Figure 11. Capacitance Variation

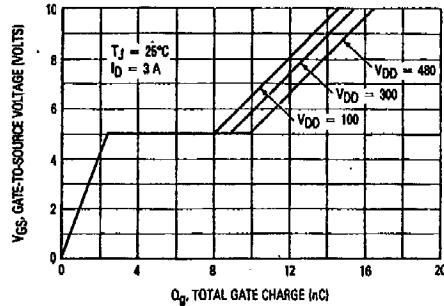


Figure 12. Gate Charge versus Gate-to-Source Voltage

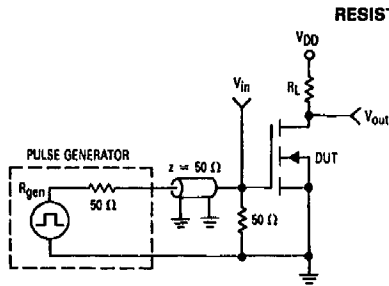


Figure 13. Switching Test Circuit

RESISTIVE SWITCHING

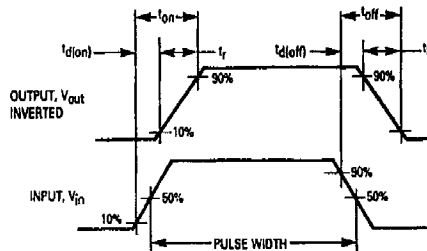


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

