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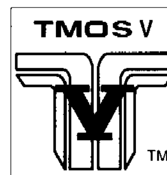
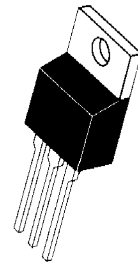
MTP50N06V

TMOS V™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

TMOS POWER FET
42 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.028 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





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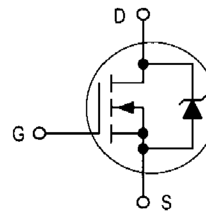

New Features of TMOS V

- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS

- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 25	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	42 30 147	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C	P_D	125 0.83	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 42 Apk, L = 0.454 µH, R_G = 25 Ω)	E_{AS}	400	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.2 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However, NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.

NJS

Quality Semi-Conductors

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	69	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.7	4.0	Vdc
Temperature Coefficient (Negative)			—	3.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 21 Adc)		$R_{DS(on)}$	—	0.025	0.028	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 42 Adc)		$V_{DS(on)}$	—	1.4	1.7	Vdc
(I_D = 21 Adc, T_J = 150°C)			—	—	1.6	
Forward Transconductance (V_{DS} = 6.25 Vdc, I_D = 20 Adc)		g_{FS}	16	23	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1644	2320	pF
Output Capacitance		C_{oss}	—	465	660	
Reverse Transfer Capacitance		C_{rss}	—	112	230	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 25 Vdc, I_D = 42 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	12	20	ns
Rise Time		t_r	—	122	250	
Turn–Off Delay Time		$t_{d(off)}$	—	64	110	
Fall Time		t_f	—	54	90	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 42 Adc, V_{GS} = 10 Vdc)	Q_T	—	47	70	nC
		Q_1	—	9	—	
		Q_2	—	21	—	
		Q_3	—	16	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 42 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.06	2.5	Vdc
	(I_S = 42 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	0.99	—	
Reverse Recovery Time (See Figure 14)	(I_S = 42 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	84	—	ns
		t_a	—	73	—	
		t_b	—	11	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.28	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)				4.5		
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH