

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

PRELIMINARY DATA

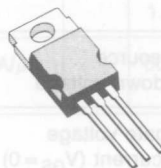
TYPE	V _{DSS}	R _{DS(on)}	I _D
MTP6N60	600 V	1.2 Ω	6 A

- HIGH VOLTAGE - 600 V FOR OFF-LINE APPLICATIONS
- ULTRA FAST SWITCHING TIMES FOR OPERATIONS AT > 100KHz
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- SWITCHING POWER SUPPLY
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make these POWER MOS ideal for very high speed switching applications. Typical uses include SMPS, uninterruptible power supplies and motor controls.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V _{DS}	Drain-source voltage (V _{GS} = 0)	600	V
V _{DGR}	Drain-gate voltage (R _{GS} = 20 KΩ)	600	V
V _{GS}	Gate-source voltage	± 20	V
I _D	Drain current (cont.) at T _c = 25°C	6	A
I _{DM}	Drain current (pulsed)	30	A
P _{tot}	Total dissipation at T _c < 25°C	125	W
	Derating factor	1	W/°C
T _{stg}	Storage temperature	- 65 to 150	°C
T _j	Max. operating junction temperature	150	°C

THERMAL DATA

$R_{thj-case}$	Thermal resistance junction-case	max	1	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	max	62.5	°C/W

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$	$V_{GS} = 0$	600		V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$	$V_{DS} = \text{Max Rating} \times 0.8$		200 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 500	nA

ON

$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 1 \text{ mA}$ $V_{DS} = V_{GS}$ $I_D = 1 \text{ mA}$ $T_c = 100^{\circ}\text{C}$		2 1.5	4.5 4	V V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ $I_D = 3 \text{ A}$			1.2	Ω
$V_{DS(on)}$	Drain-source on voltage	$V_{GS} = 10 \text{ V}$ $I_D = 6 \text{ A}$ $V_{GS} = 10 \text{ V}$ $I_D = 3 \text{ A}$ $T_c = 100^{\circ}\text{C}$			8 7.2	V V

DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} = 10 \text{ V}$ $I_D = 3 \text{ A}$		2		mho
C_{iss}	Input capacitance				1800	pF
C_{oss}	Output capacitance	$V_{DS} = 25 \text{ V}$ $f = 1 \text{ MHz}$			350	pF
C_{rss}	Reverse transfer capacitance	$V_{GS} = 0$			150	pF

SWITCHING

$t_{d(on)}$	Turn-on time	$V_{DD} = 25 \text{ V}$	$I_D = 3 \text{ A}$		60	ns
t_r	Rise time	$R_i = 50 \Omega$	$V_i = 10 \text{ V}$		150	ns
$t_{d(off)}$	Turn-off delay time				200	ns
t_f	Fall time				120	ns

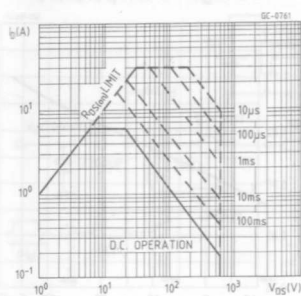
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)			6 30	A A
V_{SD}	Forward on voltage	$I_{SD} = 6\text{ A}$	$V_{GS} = 0$	1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 6\text{ A}$	$di/dt = 100\text{A}/\mu\text{s}$	600	ns

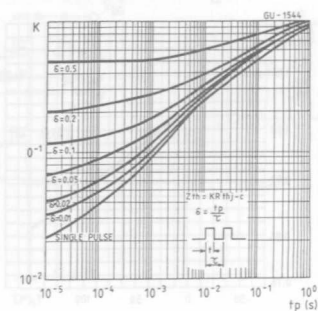
SOURCE DRAIN DIODE

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)			6 30	A A
V_{SD}	Forward on voltage	$I_{SD} = 6\text{ A}$	$V_{GS} = 0$	1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 6\text{ A}$	$di/dt = 100\text{A}/\mu\text{s}$	600	ns

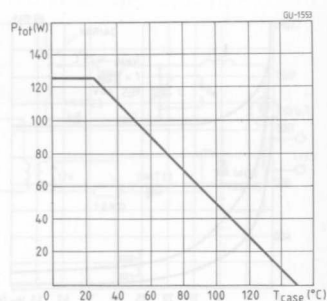
Safe operating areas



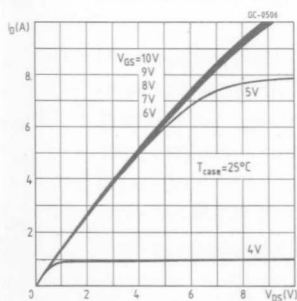
Thermal impedance



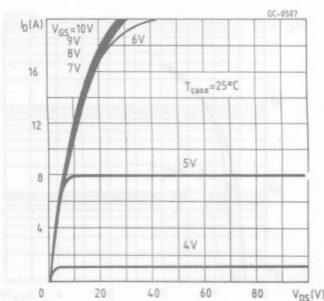
Derating curve



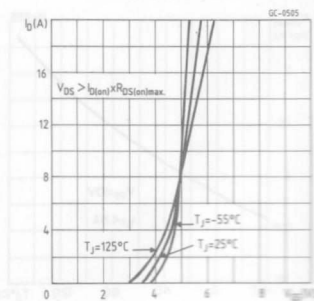
Output characteristics



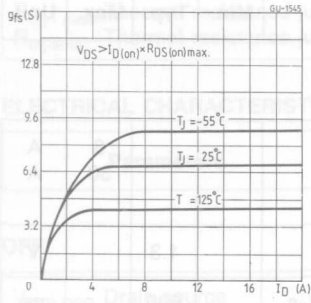
Output characteristics



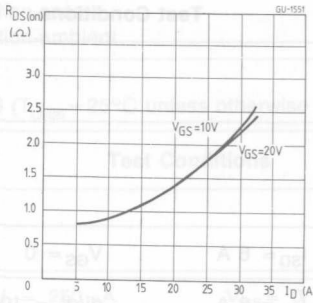
Transfer characteristics



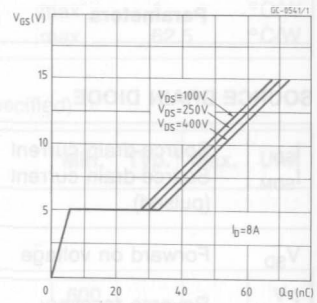
Transconductance



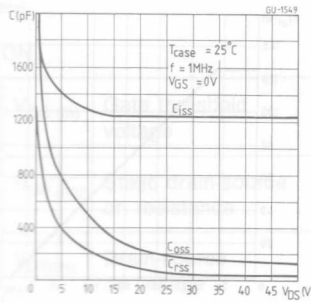
Static drain-source on resistance



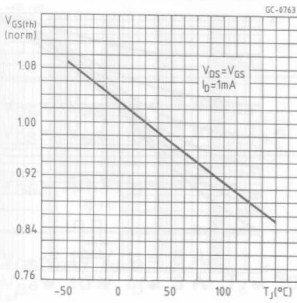
Gate charge vs gate-source voltage



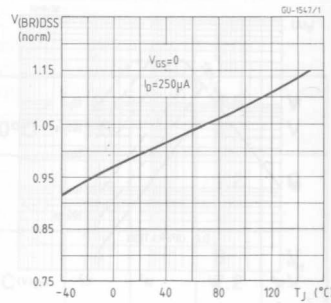
Capacitance variation



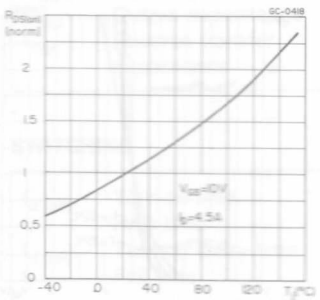
Normalized gate threshold voltage vs temperature



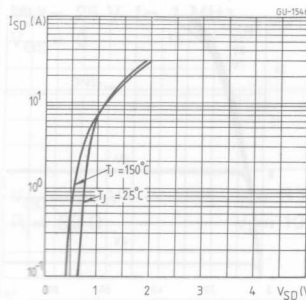
Normalized breakdown voltage vs temperature



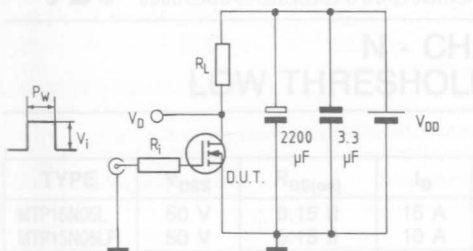
Normalized on resistance vs temperature



Source-drain diode forward characteristics



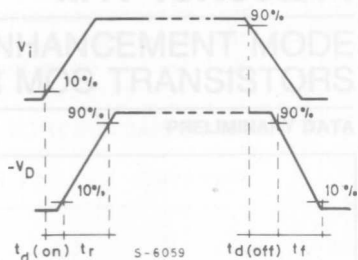
Switching times test circuit for resistive load



Pulse width $\leq 100 \mu\text{s}$
Duty cycle $\leq 2\%$

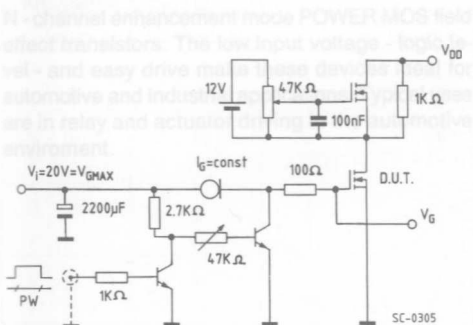
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Switching time waveforms for resistive load



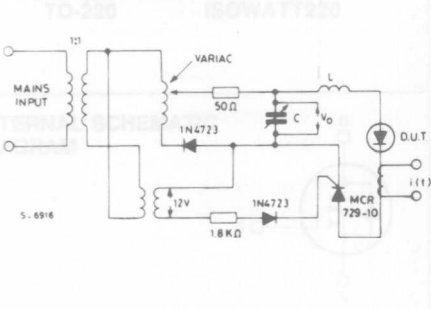
- * LOGIC LEVEL (+6V) CMOS/TTL COMPATIBLE INPUT
- * HIGH INPUT IMPEDANCE
- * ULTRA FAST SWITCHING

Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



ABSOLUTE MAXIMUM RATINGS

	TO-220 ISOWATT220	MTP15N06L MTP15N06LF	MTP15N05L MTP15N05LF
V_{DS}	Drain-source voltage ($I_{DS} = 0$)	60	50
V_{GSM}	Drain-gate voltage ($I_{DS} = 20 \text{ Kl}$)	60	50
V_{GS}	Gate-source voltage	±15	
I_D	Drain current (cont.) at $T_c = 25^\circ\text{C}$	15	10
I_D	Drain current (cont.) at $T_c = 100^\circ\text{C}$	9.5	6.3
I_{DM}	Drain current (pulsed)	40	40
P_{tot}	Total dissipation at $T_c < 25^\circ\text{C}$	75	30
λ	Dersing factor	0.6	0.24
T_{stg}	Storage temperature	-85 to 150	
T_{jmax}	Max. operating junction temperature	150	

(1) Pulse width limited by safe operating area