PRELIMINARY DATA SHEET

NEC

SILICON POWER MOS FET

NE5500179A

4.8 V OPERATION SILICON RF POWER LD-MOS FET FOR 1.9 GHz 1 W TRANSMISSION AMPLIFIERS

DESCRIPTION

The NE5500179A is an N-channel silicon power MOS FET specially designed as the transmission driver amplifier for 4.8 V GSM 1 800 and GSM 1 900 handsets. Dies are manufactured using NEC's NEWMOS technology (NEC's 0.6 μm WSi gate lateral-diffusion MOS FET) and housed in a surface mount package. The device can deliver 30.0 dBm output power with 55% power added efficiency at 1.9 GHz under the 4.8 V supply voltage, or can deliver 27 dBm output power with 50% power added efficiency at 3.5 V, respectively.

FEATURES

- High output power : P_{out} = 30.0 dBm TYP. (V_{DS} = 4.8 V, I_{Dset} = 200 mA, f = 1.9 GHz, P_{in} = 20 dBm)
- High power added efficiency : η_{add} = 55% TYP. (V_{DS} = 4.8 V, I_{Dset} = 200 mA, f = 1.9 GHz, P_{in} = 20 dBm)
- High linear gain : G_L = 14.0 dB TYP. (V_{DS} = 4.8 V, I_{Dset} = 200 mA, f = 1.9 GHz, P_{in} = 10 dBm)
- Surface mount package : 5.7 × 5.7 × 1.1 mm MAX.
- Single supply : V_{DS} = 3.0 to 6.0 V

APPLICATIONS

- Digital cellular phones : 4.8 V driver amplifier for GSM 1 800/ GSM 1 900 class 1 handsets, or 4.8 V final stage amplifier
- Digital cordless phones : 3.5 V final stage amplifier for DECT
- Others : General purpose amplifiers for 1.6 to 2.5 GHz TDMA applications

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
NE5500179A-T1	79A	R1	• 12 mm wide embossed taping • Gate pin face the perforation side of the tape • Qty 1 kpcs/reel

Remark To order evaluation samples, consult your NEC sales representative.
Part number for sample order: NE5500179A

Caution Please handle this device at static-free workstation, because this is an electrostatic sensitive device.

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ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	8.5	V
Gate to Source Voltage	V_{GSO}	5.0	V
Drain Current	I_D	0.25	A
Drain Current (Pulse Test)	I_D Note	0.5	A
Total Power Dissipation	P_{tot}	1.6	W
Channel Temperature	T_{ch}	125	°C
Storage Temperature	T_{stg}	−65 to +125	°C

Note Duty Cycle ≤ 50%, T_{on} ≤ 1 ms

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain to Source Voltage	V_{DS}		3.0	4.8	6.0	V
Gate to Source Voltage	V_{GSO}		0	2.0	3.5	V
Drain Current (Pulse Test)	I_D	Duty Cycle ≤ 50%, T_{on} ≤ 1 ms	–	340	–	mA
Input Power	P_{in}	f = 1.9 GHz, V_{DS} = 4.8 V	0	20	22	dBm

ELECTRICAL CHARACTERISTICS (T_A = +25°C)

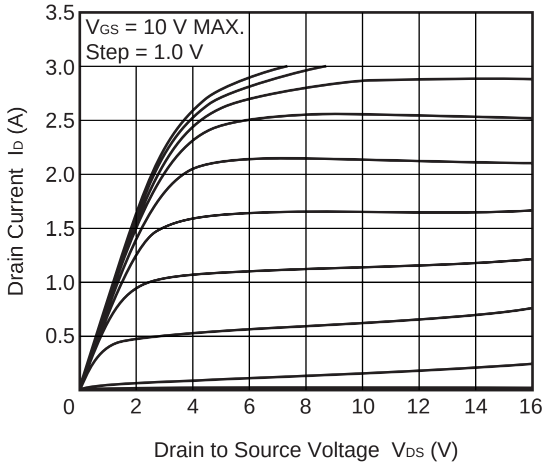
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Gate to Source Leak Current	I_{GSO}	V_{GSS} = 5.0 V	–	–	100	nA
Saturated Drain Current (Zero Gate Voltage Drain Current)	I_{DSS}	V_{DSS} = 8.5 V	–	–	100	nA
Gate Threshold Voltage	V_{th}	V_{DS} = 4.8 V, I_{DS} = 1 mA	1.0	1.45	2.0	V
Transconductance	g_m	V_{DS} = 4.8 V, I_{DS} = 250 mA	–	420	–	mS
Drain to Source Breakdown Voltage	BV_{DS}	I_{DSS} = 10 μA	20	24	–	V
Thermal Resistance	R_{th}	Channel to Case	–	10	–	°C/W
Linear Gain	G_L	f = 1.9 GHz, P_{in} = 10 dBm, V_{DS} = 4.8 V, I_{Dset} = 200 mA, **Note 1, 2**	–	14.0	–	dB
Output Power	P_{out}	f = 1.9 GHz, P_{in} = 20 dBm, V_{DS} = 4.8 V, I_{Dset} = 200 mA, **Note 1, 2**	28.5	30.0	–	dBm
Operating Current	I_{op}		–	340	–	mA
Power Added Efficiency	η_{add}		48	55	–	%

Notes 1. Peak measurement at Duty Cycle ≤ 50%, T_{on} ≤ 1 ms.

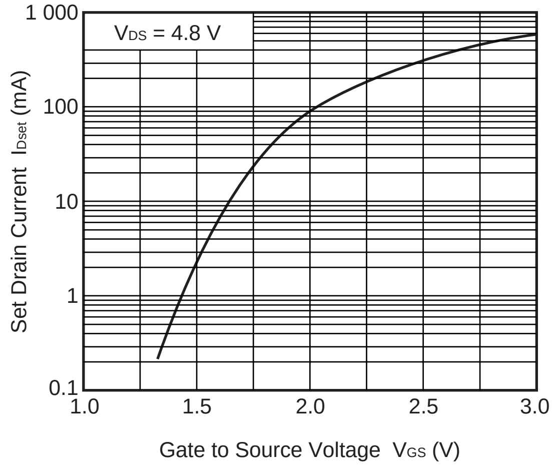
2. DC performance is 100% testing. RF performance is testing several samples per wafer. Wafer rejection criteria for standard devices is 1 reject for several samples.

TYPICAL CHARACTERISTICS (T_A = +25°C)

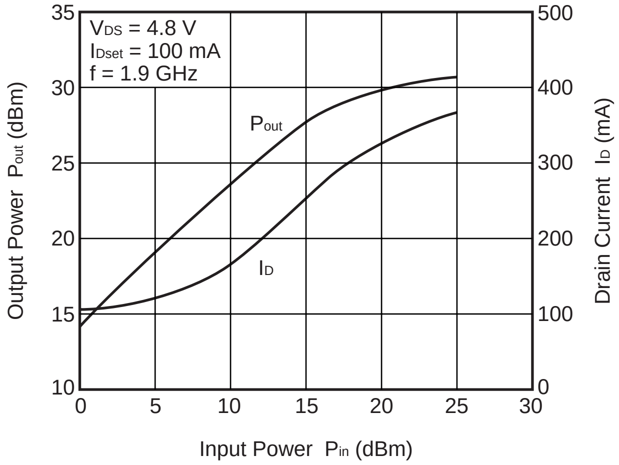
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



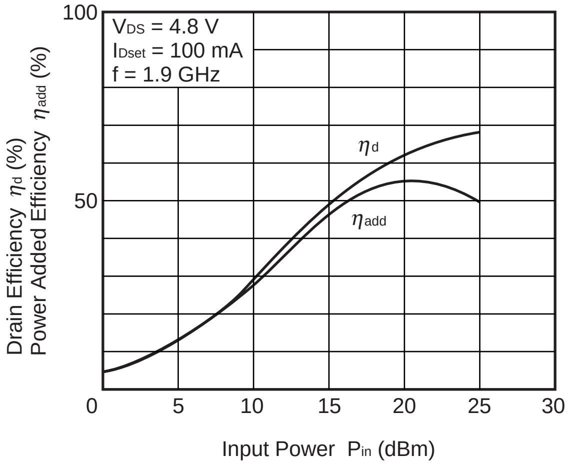
SET DRAIN CURRENT vs.
GATE TO SOURCE VOLTAGE



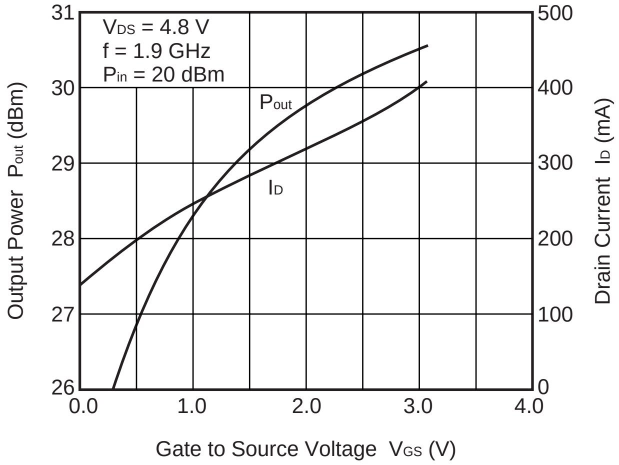
OUTPUT POWER, DRAIN CURRENT
vs. INPUT POWER



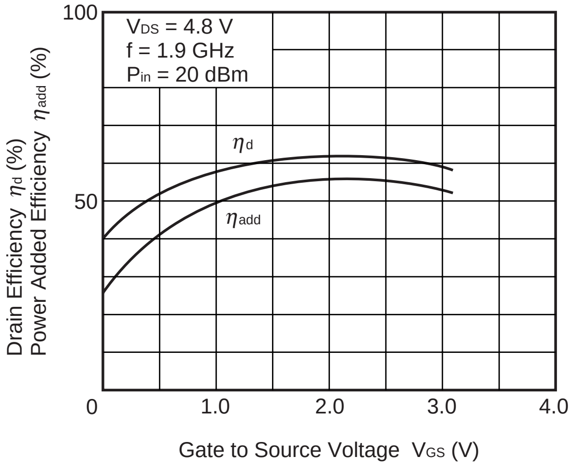
DRAIN EFFICIENCY, POWER ADDED
EFFICIENCY vs. INPUT POWER



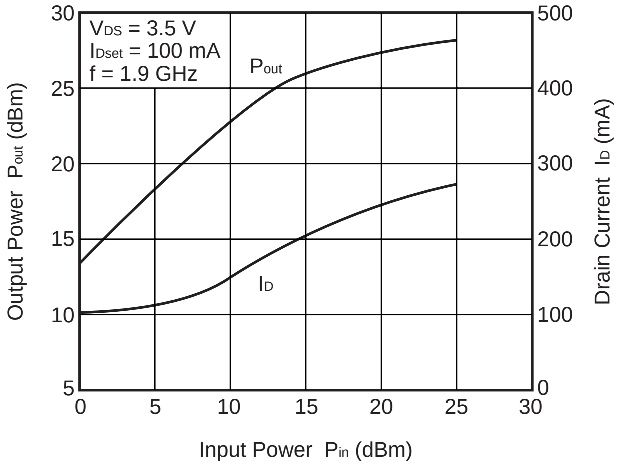
OUTPUT POWER, DRAIN CURRENT
vs. GATE TO SOURCE VOLTAGE



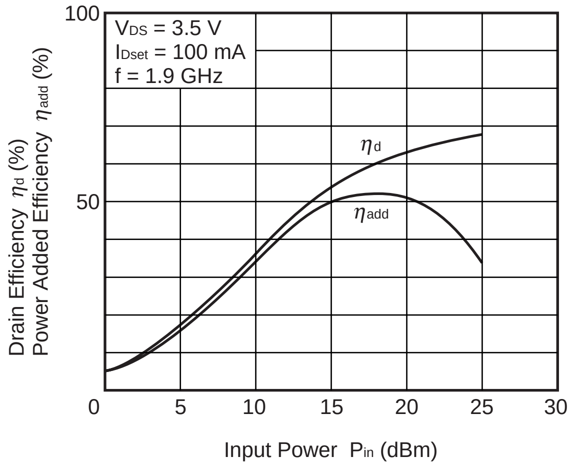
DRAIN EFFICIENCY, POWER ADDED
EFFICIENCY vs. GATE TO SOURCE VOLTAGE



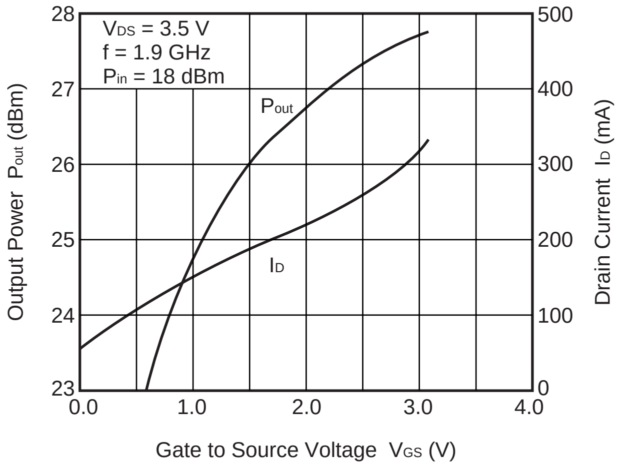
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER



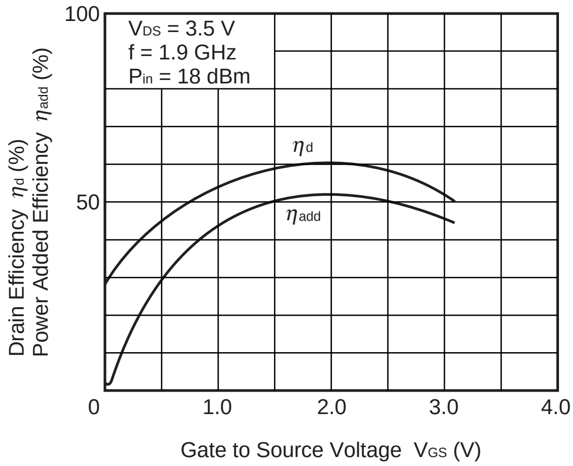
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



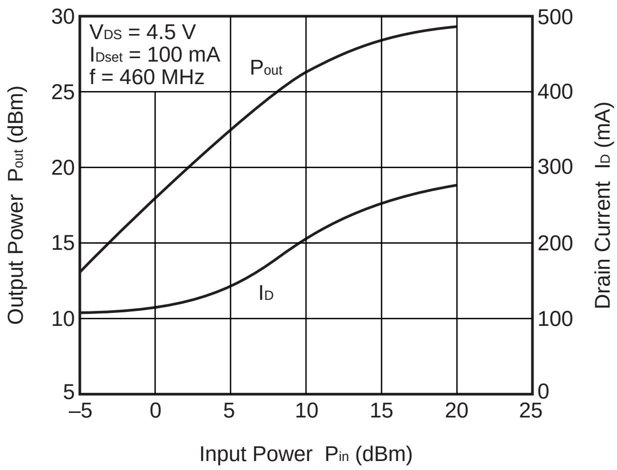
OUTPUT POWER, DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



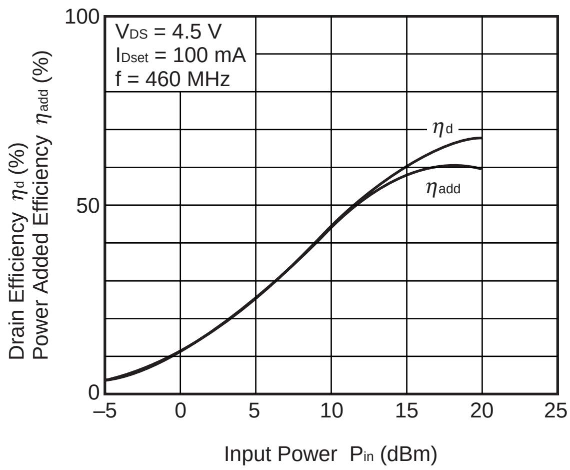
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. GATE TO SOURCE VOLTAGE



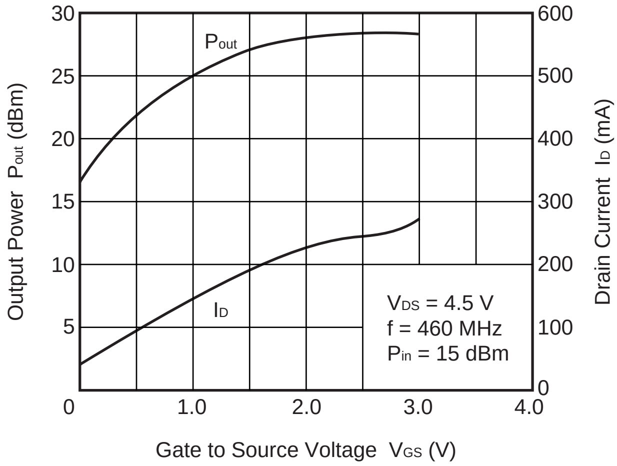
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER



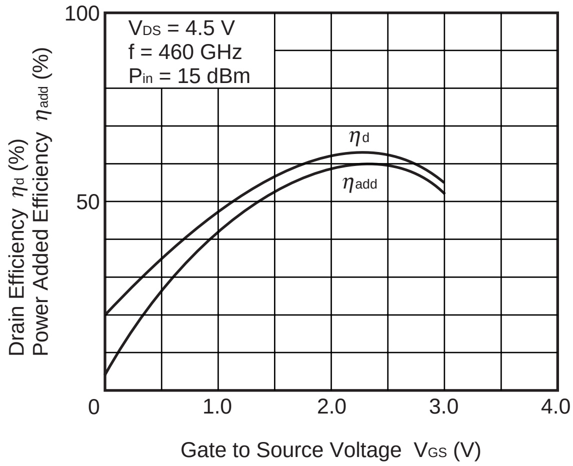
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



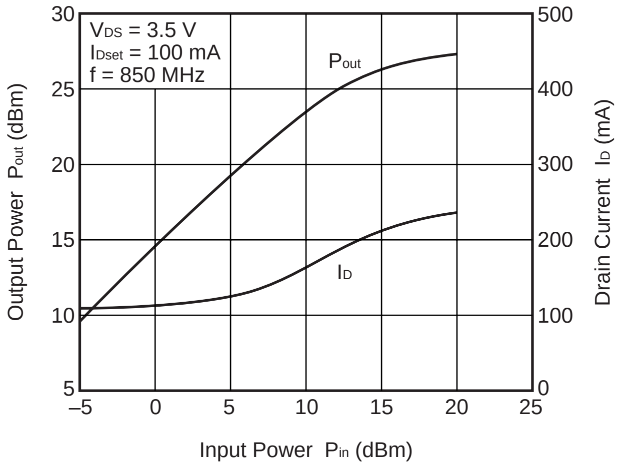
OUTPUT POWER, DRAIN CURRENT
vs. GATE TO SOURCE VOLTAGE



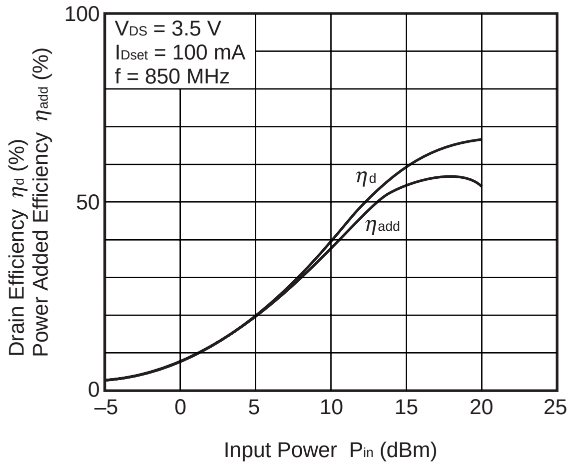
DRAIN EFFICIENCY, POWER ADDED
EFFICIENCY vs. GATE TO SOURCE VOLTAGE



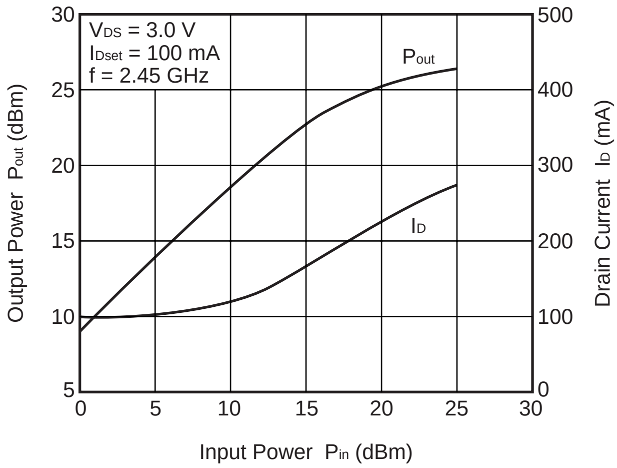
OUTPUT POWER, DRAIN CURRENT
vs. INPUT POWER



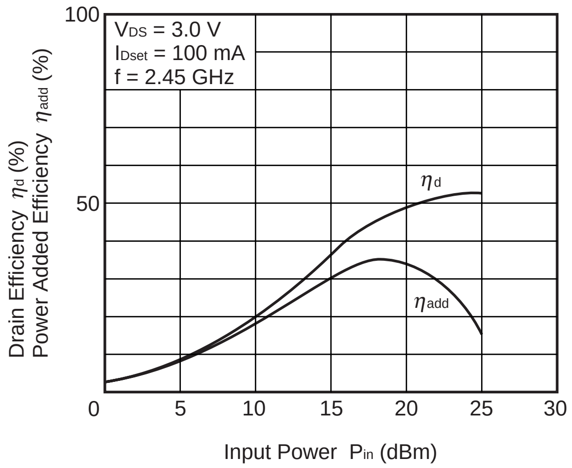
DRAIN EFFICIENCY, POWER ADDED
EFFICIENCY vs. INPUT POWER



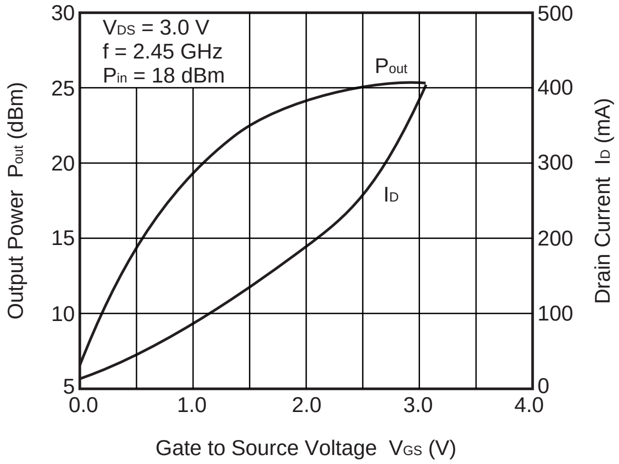
OUTPUT POWER, DRAIN CURRENT
vs. INPUT POWER



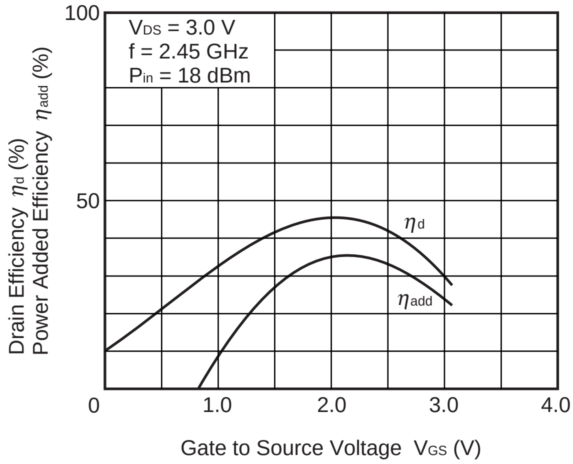
DRAIN EFFICIENCY, POWER ADDED
EFFICIENCY vs. INPUT POWER



OUTPUT POWER, DRAIN CURRENT
vs. GATE TO SOURCE VOLTAGE



DRAIN EFFICIENCY, POWER ADDED
EFFICIENCY vs. GATE TO SOURCE VOLTAGE



Remark The graphs indicate nominal characteristics.

S-PARAMETERS

Test Conditions: V_{DS} = 4.8 V, I_{Dset} = 100 mA

Frequency	S11		S21			S12			S22		MAG Note	MSG Note	K
GHz	MAG.	ANG.	dB	MAG.	ANG.	dB	MAG.	ANG.	MAG.	ANG.	dB	dB	
0.1	0.844	−69.6	25.2	18.11	135.5	−28.5	0.037	48.2	0.517	−85.0		26.8	0.00
0.2	0.792	−107.8	21.7	12.12	112.3	−26.1	0.049	23.2	0.569	−120.7		23.9	0.06
0.3	0.757	−127.4	18.7	8.58	98.8	−25.5	0.052	10.8	0.598	−136.5		22.1	0.08
0.4	0.747	−138.7	16.4	6.58	89.4	−25.7	0.052	3.3	0.618	−144.8		21.0	0.11
0.5	0.746	−146.2	14.5	5.28	82.1	−25.7	0.052	−4.1	0.641	−149.5		20.1	0.13
0.6	0.751	−151.8	12.7	4.32	76.2	−26.0	0.050	−8.9	0.660	−153.4		19.3	0.18
0.7	0.756	−155.6	11.3	3.68	70.9	−26.3	0.048	−12.6	0.681	−156.2		18.8	0.22
0.8	0.772	−159.5	9.9	3.12	65.9	−26.4	0.048	−17.0	0.696	−158.9		18.1	0.23
0.9	0.777	−162.3	8.8	2.75	61.3	−26.9	0.045	−22.1	0.715	−161.0		17.9	0.28
1.0	0.785	−165.0	7.6	2.40	58.2	−27.2	0.043	−21.9	0.732	−162.9		17.4	0.33
1.1	0.796	−167.7	6.7	2.17	53.7	−27.8	0.040	−26.9	0.749	−164.9		17.2	0.35
1.2	0.804	−169.9	5.7	1.91	51.4	−28.3	0.038	−29.2	0.763	−166.9		17.0	0.42
1.3	0.814	−172.4	4.8	1.74	46.4	−28.7	0.036	−30.5	0.776	−169.1		16.8	0.45
1.4	0.820	−174.6	4.0	1.58	44.3	−29.0	0.035	−31.4	0.789	−171.0		16.5	0.48
1.5	0.827	−176.8	3.2	1.45	39.7	−28.9	0.035	−36.6	0.803	−172.7		16.1	0.44
1.6	0.832	−179.6	2.5	1.33	38.4	−30.0	0.031	−38.5	0.808	−175.0		16.3	0.62
1.7	0.833	177.9	1.5	1.19	34.6	−30.5	0.030	−38.3	0.814	−176.7		16.0	0.78
1.8	0.846	175.6	1.1	1.13	31.6	−31.0	0.028	−38.7	0.829	−179.2		16.1	0.70
1.9	0.843	172.9	0.2	1.02	28.3	−31.8	0.025	−38.1	0.834	178.7		16.0	0.98
2.0	0.850	170.3	0.0	0.99	27.1	−32.2	0.024	−40.9	0.840	176.5		16.1	0.97
2.1	0.851	167.1	−1.0	0.89	23.3	−33.5	0.021	−42.9	0.842	174.4	12.4		1.42
2.2	0.854	165.1	−1.6	0.83	21.4	−34.1	0.019	−48.0	0.847	172.1	11.7		1.62
2.3	0.861	162.3	−2.4	0.75	16.9	−35.1	0.017	−43.6	0.856	169.1	10.9		1.88
2.4	0.857	159.5	−2.3	0.76	15.5	−34.9	0.017	−40.8	0.866	167.0	11.5		1.68
2.5	0.870	156.6	−3.4	0.67	13.8	−36.1	0.015	−49.0	0.862	164.7	10.2		2.20
2.6	0.870	153.9	−3.6	0.65	12.0	−35.8	0.016	−36.8	0.865	162.0	10.1		2.13
2.7	0.867	151.6	−5.0	0.56	9.0	−39.4	0.010	−33.0	0.866	159.1	7.8		4.44
2.8	0.870	148.9	−4.8	0.57	3.9	−39.9	0.010	−43.4	0.879	156.7	8.6		3.96
2.9	0.873	146.5	−5.6	0.52	4.7	−42.4	0.007	−18.3	0.879	154.5	7.6		6.01
3.0	0.882	143.9	−5.7	0.51	2.7	−41.3	0.008	−15.0	0.885	152.0	8.2		4.60

Note When K ≥ 1, the MAG (Maximum Available Gain) is used. $\text{MAG} = \left|\frac{S_{21}}{S_{12}}\right|\left(K - \sqrt{(K^2 - 1)}\right)$

When K < 1, the MSG (Maximum Stable Gain) is used. $\text{MSG} = \left|\frac{S_{21}}{S_{12}}\right|$, $K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 \cdot |S_{12}| \cdot |S_{21}|}$,

$\Delta = S_{11} \cdot S_{22} - S_{21} \cdot S_{12}$

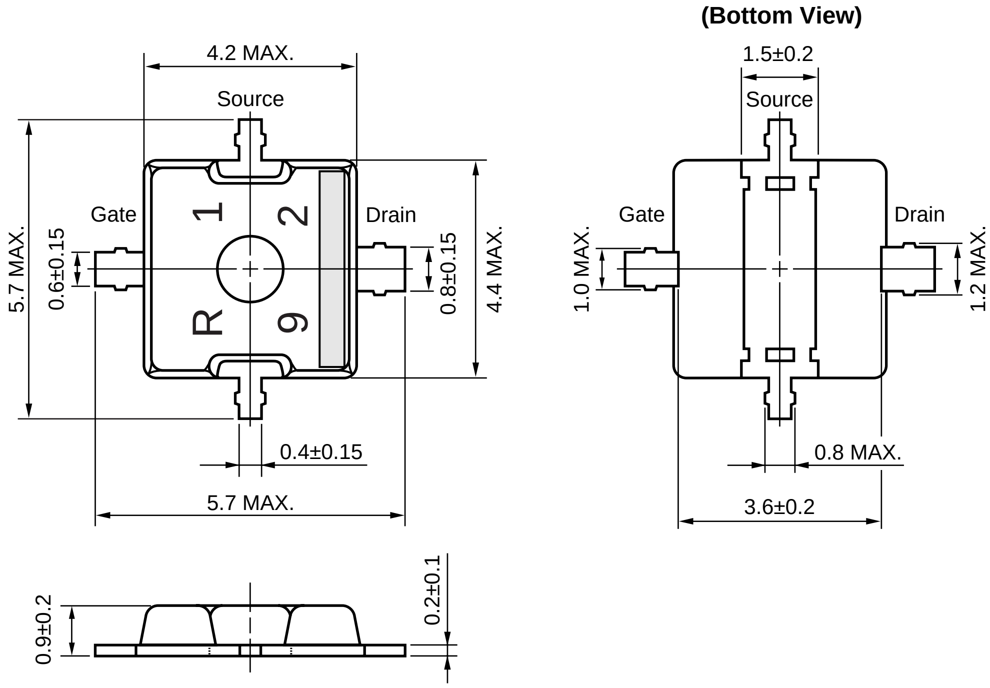
LARGE SIGNAL IMPEDANCE (V_{DS} = 4.8 V, I_{Dset} = 100 mA, P_{in} = 20 dBm)

f (GHz)	Z_{in} (Ω)	Z_{OL} (Ω) Note
1.9	TBD	TBD

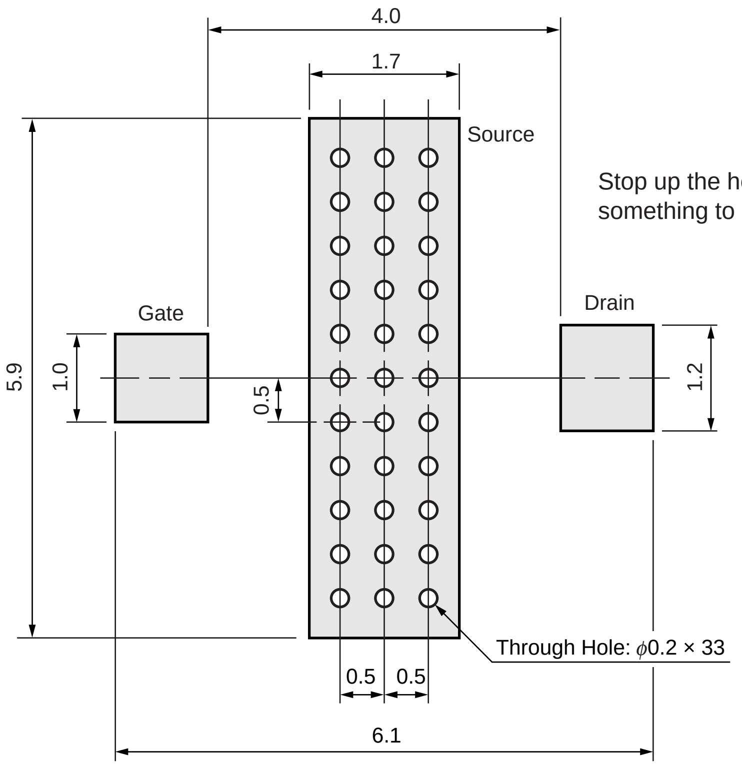
Note Z_{OL} is the conjugate of optimum load impedance at given voltage, idling current, input power and frequency.

PACKAGE DIMENSIONS

79A (UNIT: mm)



79A PACKAGE RECOMMENDED P.C.B. LAYOUT (UNIT: mm)



RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below, Time: 30 seconds or less (at 210°C or higher), Count: 2 times or less, Exposure: limit: None [Note]	IR35-00-2
Partial Heating	Pin temperature: 260°C or below, Time: 5 seconds or less (per pin row) Exposure: limit: None [Note]	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

[MEMO]