SD5000/5400 Series

N-Channel Lateral DMOS FETs

SD5000I SD5400CY
SD5000N SD5401CY
SD5001N

Product Summary

Part Number	$V_{(BR)DS}$ Min (V)	$V_{GS(th)}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD5000I	20	1.5	70 @ V_{GS} = 5 V	0.5	2
SD5000N	20	1.5	70 @ V_{GS} = 5 V	0.5	2
SD5001N	10	1.5	70 @ V_{GS} = 5 V	0.5	2
SD5400CY	20	1.5	75 @ V_{GS} = 5 V	0.5	2
SD5401CY	10	1.5	75 @ V_{GS} = 5 V	0.5	2

For applications information see AN301, page 33.

Features

- Quad SPST Switch with Zener Input Protection
- Low Interelectrode Capacitance and Leakage
- Ultra-High Speed Switching—t_{ON}: 1 ns
- Ultra-Low Reverse Capacitance: 0.2 pF
- Low Guaranteed r_{DS} @ 5 V
- Low Turn-On Threshold Voltage

Benefits

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- Video Switch
- Multiplexer
- DAC Deglitchers
- High-Speed Driver

Description

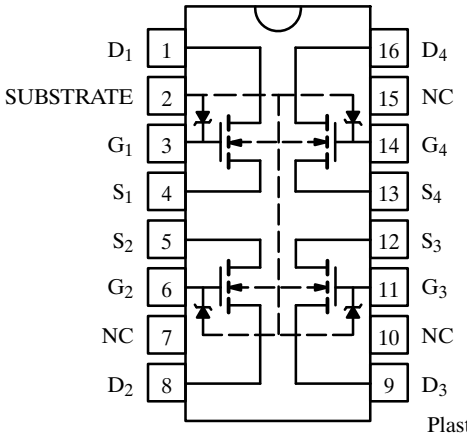
The SD5000/5400 series of monolithic switches features four individual double-diffused enhancement-mode MOSFETs built on a common substrate. These bidirectional devices provide low on-resistance and low interelectrode capacitances to minimize insertion loss and crosstalk.

Built on Siliconix' proprietary DMOS process, the SD5000/5400 series utilizes lateral construction to achieve low capacitance and ultra-fast switching speeds. For manufacturing reliability, these devices feature poly-silicon gates protected by Zener diodes.

The SD5000/5400 are rated to handle ±10-V analog signals, while the SD5001/5401 are rated for ±5-V signals.

For similar products packaged in TO-206AF (TO-72) and TO-253 (SOT-143) see the SD211DE/SST211 series.

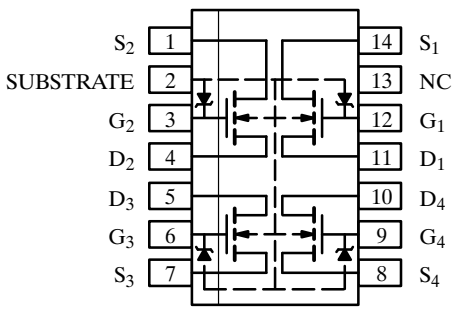
Dual-In-Line



Top View

Plastic: SD5000N
SD5001N
Sidebraze: SD5000I

Narrow Body SOIC



Top View

SD5400CY
SD5401CY

SD5000/5400 Series

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Gate-Drain, Gate-Source Voltage (SD5000, SD5400) +30 V/−25 V
(SD5001, SD5401) +25 V/−15 V

Gate-Substrate Voltage (SD5000, SD5400) ..... +30 V/−0.3 V
(SD5001, SD5401) ..... +25 V/−0.3 V

Drain-Source Voltage (SD5000, SD5400) ..... 20 V
(SD5001, SD5401) ..... 10 V

Drain-Source-Substrate Voltage (SD5000, SD5400) ..... 25 V
(SD5001, SD5401) ..... 15 V

Drain Current ..... 50 mA

Lead Temperature ($^1/_{16}$" from case for 10 seconds) ..... 300°C

Storage Temperature ..... −65 to 150°C

Operating Junction Temperature ..... −55 to 150°C

Power Dissipation[a, b]: (Package) ..... 500 mW
(Each Device) ..... 300 mW

Notes:
a. SD5000/SD5001 derate 5 mW/°C above 25°C
b. SD5400/SD5401 derate 4 mW/°C above 25°C

Specifications[a]

Parameter	Symbol[b]	Test Conditions[b]		Typ[c]	Limits SD5000 SD5400 Min	Limits SD5000 SD5400 Max	Limits SD5001 SD5401 Min	Limits SD5001 SD5401 Max	Unit
Static									
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA		30	20		10		V
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		22	20		10		V
Drain-Substrate Breakdown Voltage	$V_{(BR)DBO}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source Open		35	25		15		V
Source-Substrate Breakdown Voltage	$V_{(BR)SBO}$	$V_{GB} = 0$ V, $I_S = 10$ µA, Drain Open		35	25		15		V
Drain-Source Leakage	$I_{DS(off)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4				10	nA
			$V_{DS} = 15$ V	0.7					nA
			$V_{DS} = 20$ V	0.9		10			nA
Source-Drain Leakage	$I_{SD(off)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5				10	nA
			$V_{SD} = 15$ V	0.8					nA
			$V_{SD} = 20$ V	1		10			nA
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = 30$V		0.01		100		100	
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1$ µA, $V_{SB} = 0$ V		0.8	0.1	1.5	0.1	1.5	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{SB} = 0$ V, $I_D = 1$ mA	SD5000 Series $V_{GS} = 5$ V	58		70		70	Ω
			SD5400 Series $V_{GS} = 5$ V	60		75		75	Ω
			$V_{GS} = 10$ V	38					Ω
			$V_{GS} = 15$ V	30					Ω
			$V_{GS} = 20$ V	26					Ω
Resistance Match	$\Delta r_{DS(on)}$		$V_{GS} = 5$ V	1		5		5	Ω
Dynamic									
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, f = 1 kHz	SD5000 Series	12	10		10		mS
			SD5400 Series	11	9		9		mS
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, f = 1 MHz, $V_{GS} = V_{BS} = -15$ V	SD5000 Series	2.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		2		2	pF
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5		5	pF
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5	pF
Crosstalk		f= 3 kHz		−107					dB

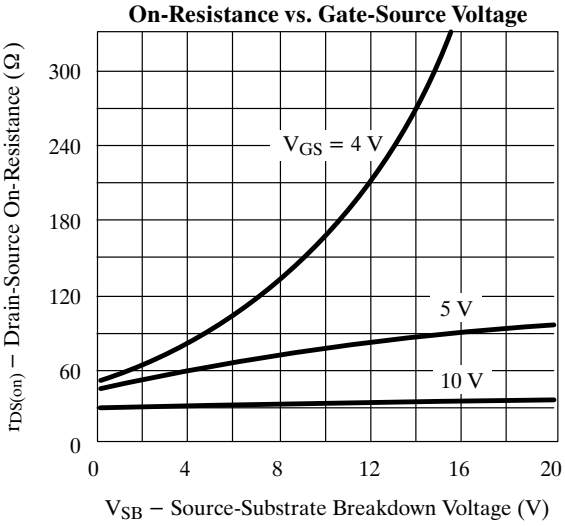
Specifications[a]

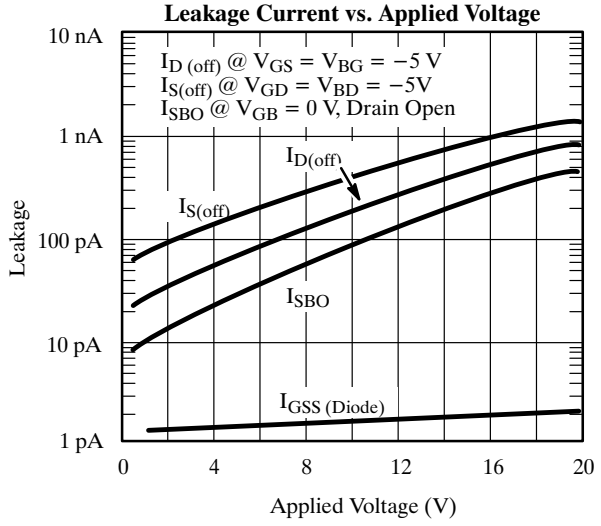
Parameter	Symbol[b]	Test Conditions[b]	Typ[c]	Limits SD5000 SD5400 Min	Limits SD5000 SD5400 Max	Limits SD5001 SD5401 Min	Limits SD5001 SD5401 Max	Unit
Switching								
Turn-On Time	$t_{d(on)}$	V_{SB} = 5 V, V_{IN} 0 to 5 V, R_G = 25 Ω V_{DD} = 5 V, R_L = 680 Ω	0.5		1		1	ns
	t_r		0.6		1		1	
Turn-Off Time	$t_{d(off)}$		2					
	t_f		6					

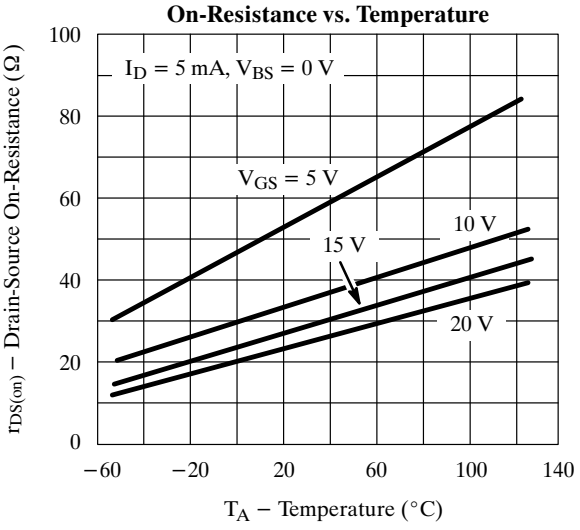
Notes:
a. T_A = 25°C unless otherwise noted.
b. B is the body (substrate) and $V_{(BR)}$ is breakdown.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

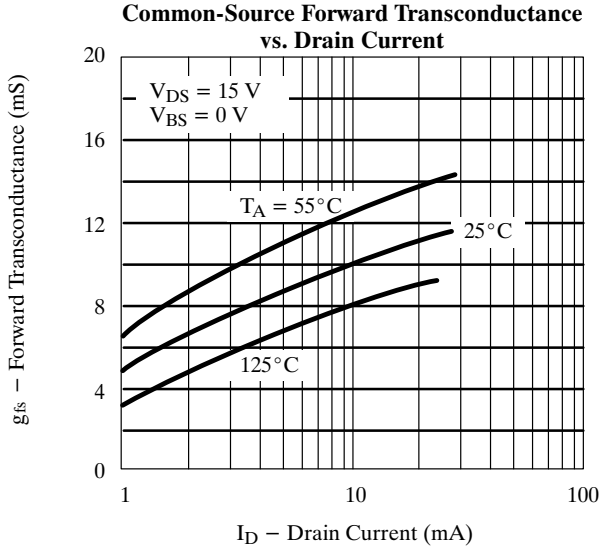
DMCA

Typical Characteristics





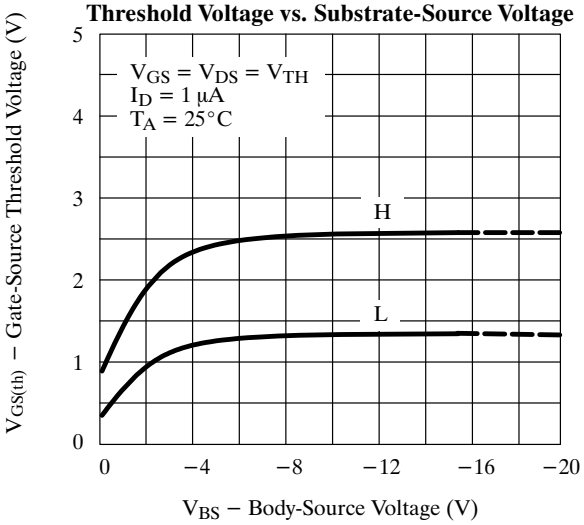




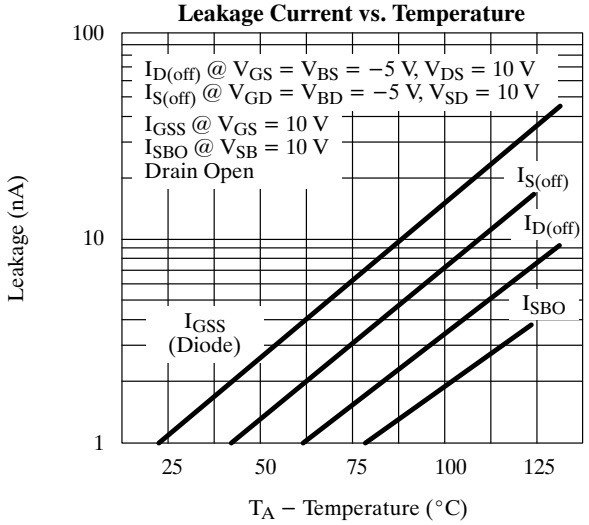
SD5000/5400 Series

Typical Characteristics (Cont'd)

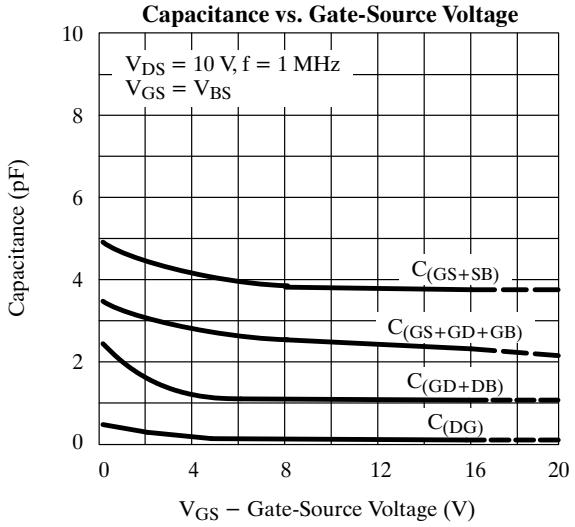
Threshold Voltage vs. Substrate-Source Voltage



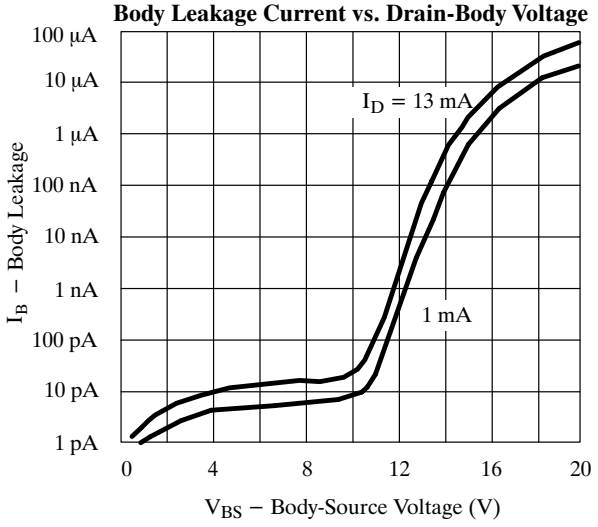
Leakage Current vs. Temperature



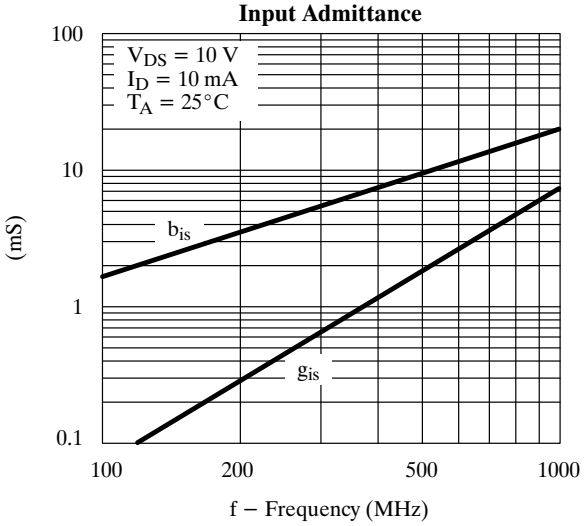
Capacitance vs. Gate-Source Voltage



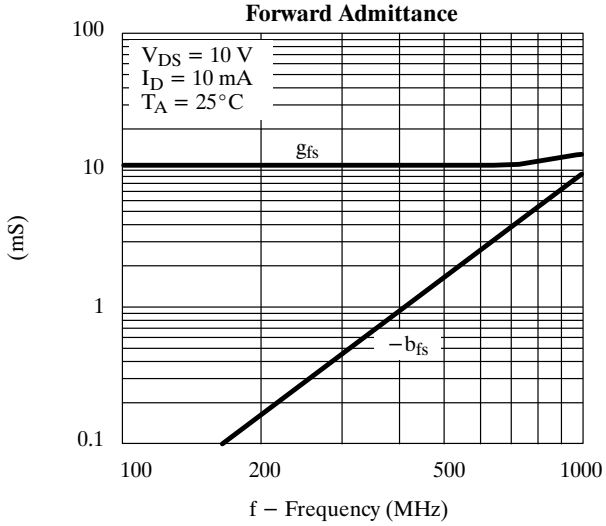
Body Leakage Current vs. Drain-Body Voltage



Input Admittance

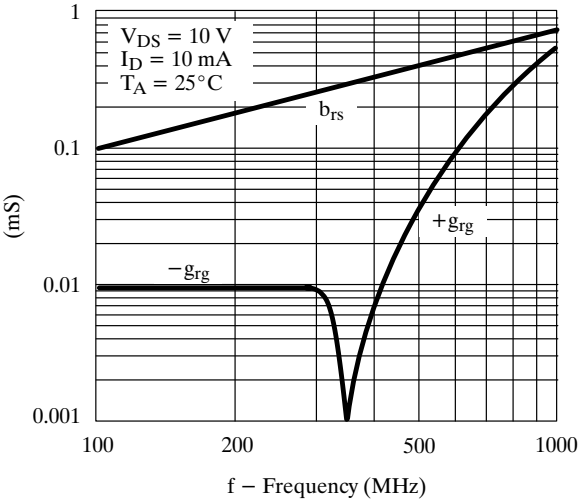


Forward Admittance

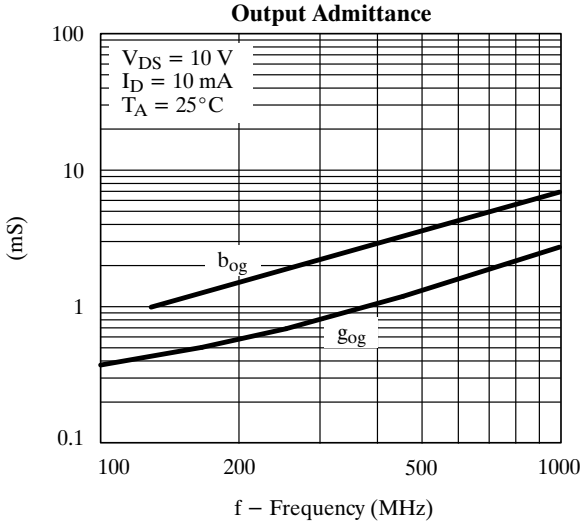


Typical Characteristics (Cont'd)

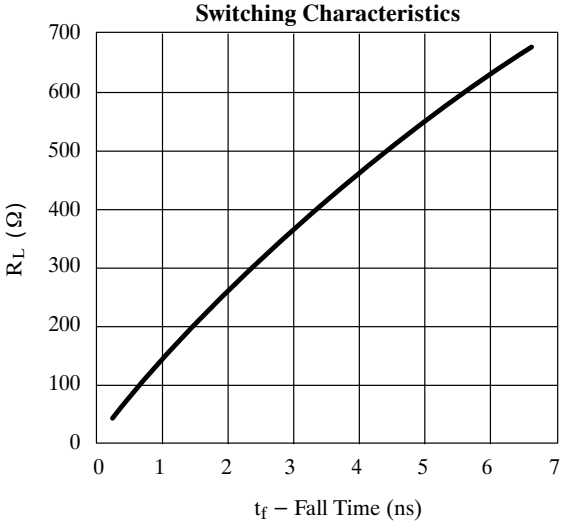
Reverse Admittance



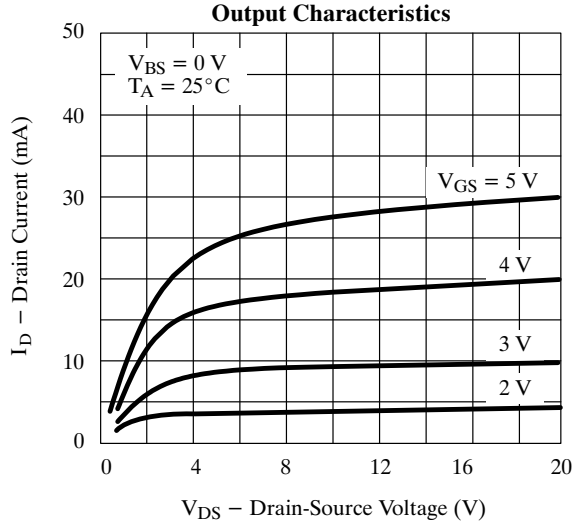
Output Admittance



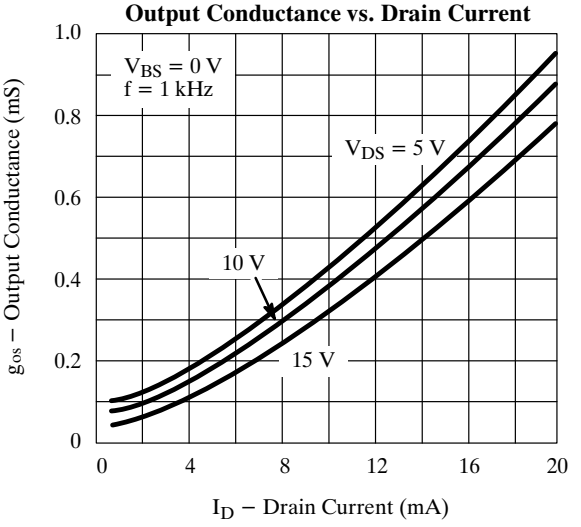
Switching Characteristics



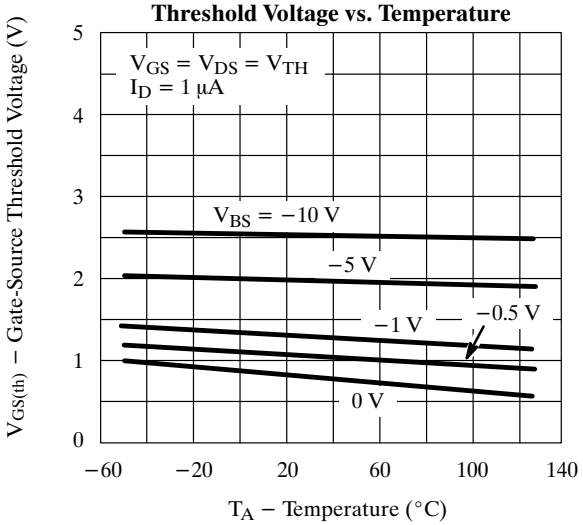
Output Characteristics



Output Conductance vs. Drain Current



Threshold Voltage vs. Temperature



SD5000/5400 Series

Switching Time Test Circuit