SGS-THOMSON MICROELECTRONICS

# SGSP201

## N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

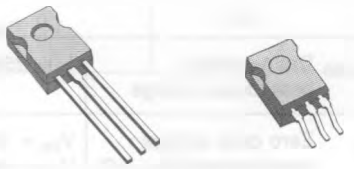
| TYPE | $V_{DSS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| SGSP201 | 100 V | 1.4 Ω | 2.0 A |

- HIGH SPEED SWITCHING APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

**INDUSTRIAL APPLICATIONS:**

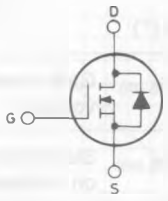
- GENERAL PURPOSE SWITCHING

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include general purpose low voltage switching, solenoid driving, motor and lamp control, switching power supplies, and driving, bipolar power switching transistors.



SOT-82 OPTION SOT-194

**INTERNAL SCHEMATIC DIAGRAM**




### ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage ($V_{GS} = 0$) | 100 | V |
| $V_{DGR}$ | Drain-gate voltage ($R_{GS} = 20$ KΩ) | 100 | V |
| $V_{GS}$ | Gate-source voltage | ±20 | V |
| $I_D$ | Drain current (cont.) at $T_c = 25°C$ | 2.0 | A |
| $I_D$ | Drain current (cont.) at $T_c = 100°C$ | 1.2 | A |
| $I_{DM}$ (*) | Drain current (pulsed) | 6 | A |
| $I_{DLM}$ (*) | Drain inductive current, clamped | 6 | A |
| $P_{tot}$ | Total dissipation at $T_c < 25°C$ | 18 | W |
| | Derating factor | 0.144 | W/°C |
| $T_{stg}$ | Storage temperature | – 65 to 150 | °C |
| $T_j$ | Max. operating junction temperature | 150 | °C |

(*) Pulse width limited by safe operating area

## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | max | 6.95 | °C/W |
| $T_L$ | Maximum lead temperature for soldering purpose | | 275 | °C |

## ELECTRICAL CHARACTERISTICS ($T_{case}$ = 25°C unless otherwise specified)

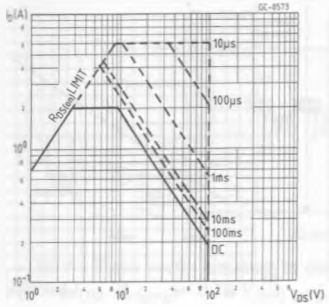
| Parameters | | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **OFF** | | | | | | |
| $V_{(BR)\ DSS}$ | Drain-source breakdown voltage | $I_D$ = 250 μA $V_{GS}$ = 0 | 100 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = Max Rating<br>$V_{DS}$ = Max Rating x 0.8 $T_c$ = 125°C | | | 250<br>1000 | μA<br>μA |
| $I_{GSS}$ | Gate-body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ±20 V | | | ±100 | nA |
| **ON (*)** | | | | | | |
| $V_{GS\ (th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$ $I_D$ = 250 μA | 2 | | 4 | V |
| $R_{DS\ (on)}$ | Static drain-source on resistance | $V_{GS}$ = 10 V $I_D$ = 1.2 A<br>$V_{GS}$ = 10 V $I_D$ = 1.2 A $T_c$ = 100°C | | | 1.4<br>2.8 | Ω<br>Ω |
| **DYNAMIC** | | | | | | |
| $g_{fs}$ | Forward transconductance | $V_{DS}$ = 25 V $I_D$ = 1.2 A | 0.5 | | | mho |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS}$ = 25 V f = 1 MHz<br>$V_{GS}$ = 0 | | 90 | 125<br>45<br>30 | pF<br>pF<br>pF |
| **SWITCHING** | | | | | | |
| $t_{d\ (on)}$<br>$t_r$<br>$t_{d\ (off)}$<br>$t_f$ | Turn-on time<br>Rise time<br>Turn-off delay time<br>Fall time | $V_{DD}$ = 50 V $I_D$ = 1.2 A<br>$V_i$ = 10 V $R_i$ = 4.7 Ω<br>(see test circuit) | | 10<br>20<br>15<br>15 | 15<br>30<br>20<br>20 | ns<br>ns<br>ns<br>ns |

## ELECTRICAL CHARACTERISTICS (Continued)

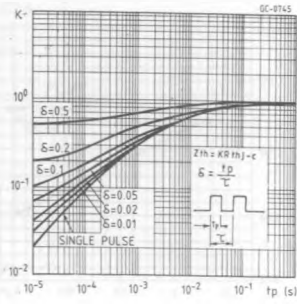
| Parameters | | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **SOURCE DRAIN DIODE** | | | | | | | |
| $I_{SD}$<br>$I_{SDM}$ (*) | Source-drain current<br>Source-drain current (pulsed) | | | | | 2.0<br>6 | A<br>A |
| $V_{SD}$ | Forward on voltage | $I_{SD}$ = 2.0 A | $V_{GS}$ = 0 | | | 1.35 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 2.0 A<br>di/dt = 25 A/$\mu$s | $V_{GS}$ = 0 | | 90 | | ns |

(*) Pulsed: Pulse duration = 300 $\mu$s, duty cycle 1.5%
(°) Pulse width limited by safe operating area

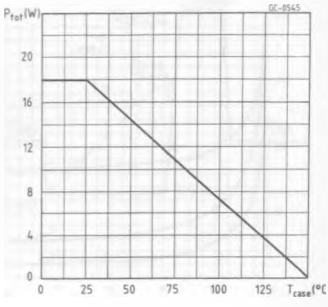
Safe operating areas



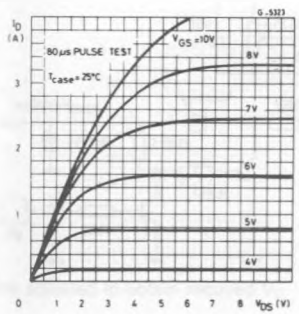

Thermal impedance



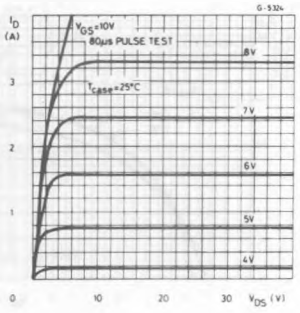

Derating curve



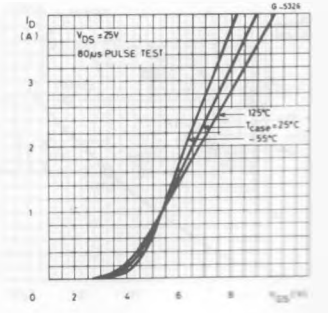

Output characteristics



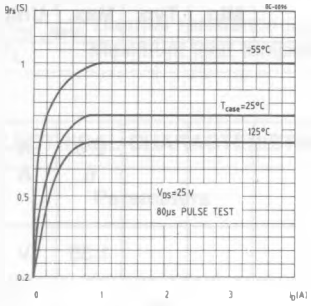

Output characteristics



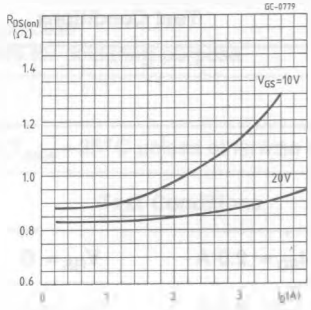

Transfer characteristics



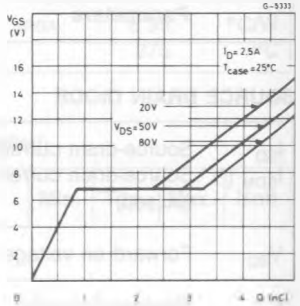
Transconductance



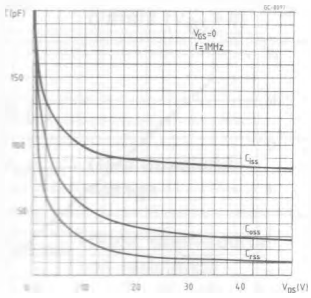

Static drain-source on resistance



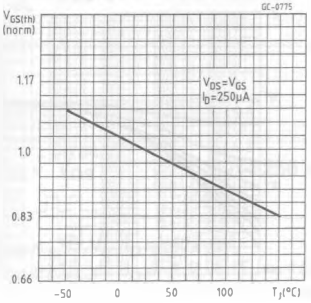

Gate charge vs gate-source voltage



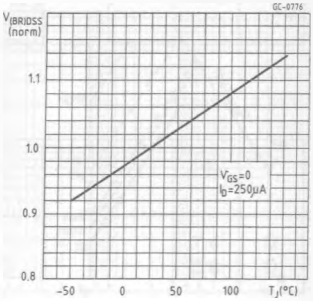

Capacitance variation



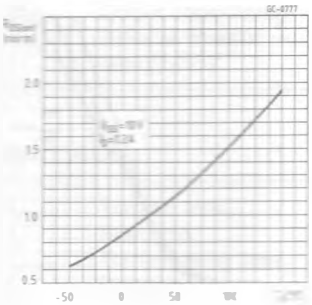

Normalized gate threshold voltage vs temperature



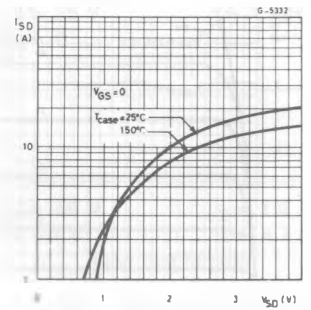

Normalized breakdown voltage vs temperature



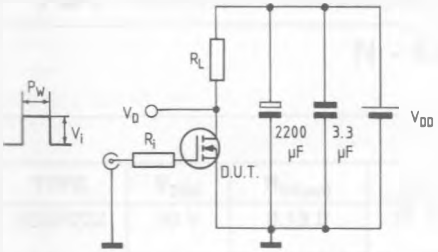

Normalized on resistance vs temperature




Source-drain diode forward characteristics

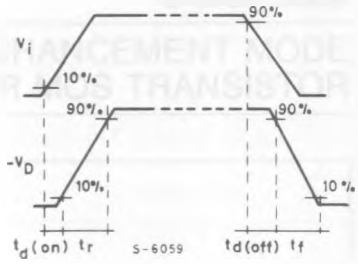


Switching times test circuit for resistive load

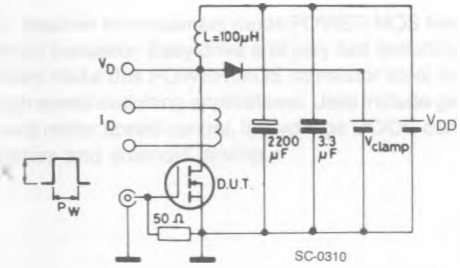



Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

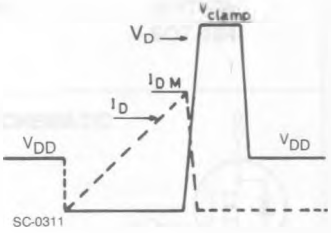



Clamped inductive load test circuit

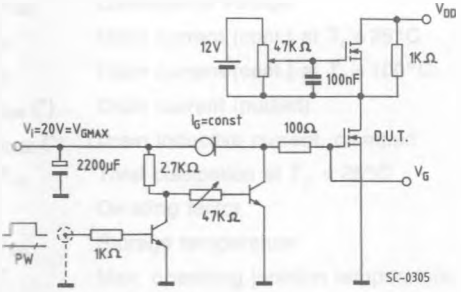



$V_i$ = 12 V - Pulse width: adjusted to obtain specified $I_{DM}$, $V_{clamp}$ = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms




Gate charge test circuit




PW adjusted to obtain required $V_G$

Body-drain diode $t_{rr}$ measurement
Jedec test circuit