SGS-THOMSON MICROELECTRONICS

SGSP311

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

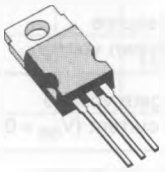
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP311	100 V	0.3 Ω	11 A

- HIGH SPEED SWITCHING APPLICATIONS
- 100V FOR DC/DC CONVERTERS
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- SWITCHING MODE POWER SUPPLIES
- STEPPER MOTOR CONTROL

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical uses include DC/DC converters, stepper motors and solenoid drives.



T0-220

INTERNAL SCHEMATIC DIAGRAM

ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	100	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20$ KΩ)	100	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c = 25°C$	11	A
I_D	Drain current (cont.) at $T_c = 100°C$	7	A
I_{DM} (•)	Drain current (pulsed)	30	A
P_{tot}	Total dissipation at $T_c < 25°C$	75	W
	Derating factor	0.6	W/°C
T_{stg}	Storage temperature	– 65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area
◆ Introduced in 1989 week 1

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.67	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

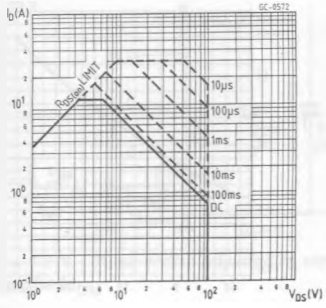
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 5.5 A V_{GS} = 10 V I_D = 5.5 A T_c = 100°C			0.3 0.6	Ω Ω
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C	11			A
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 5.5 A	2			mho
C_{iss}	Input capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		375	480	pF
C_{oss}	Output capacitance				230	pF
C_{rss}	Reverse transfer capacitance				110	pF
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 50 V I_D = 5.5 A		15	20	ns
t_r	Rise time	V_i = 10 V R_i = 4.7 Ω		40	55	ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		40	55	ns
t_f	Fall time			20	30	ns

ELECTRICAL CHARACTERISTICS (Continued)

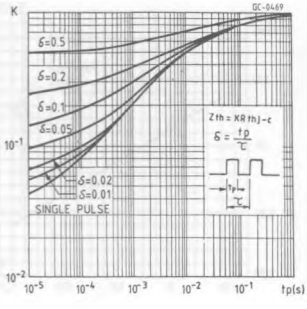
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)					11 44	A A
V_{SD}	Forward on voltage	I_{SD} = 11 A	V_{GS} = 0			1.35	V
t_{rr}	Reverse recovery time	I_{SD} = 11 A di/dt = 25 A/μs	V_{GS} = 0		140		ns

(•) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

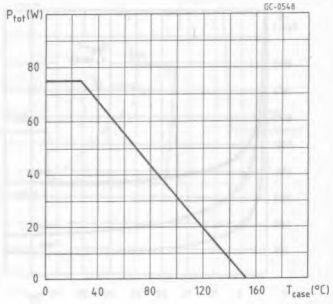
Safe operating areas



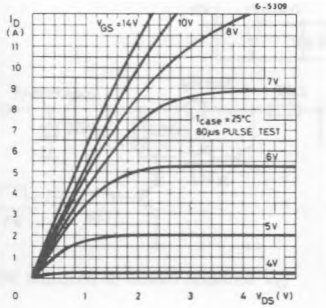
Thermal impedance



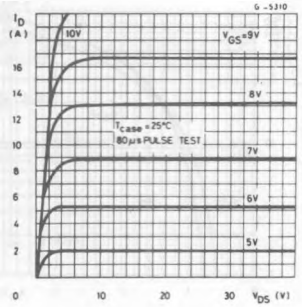
Derating curve



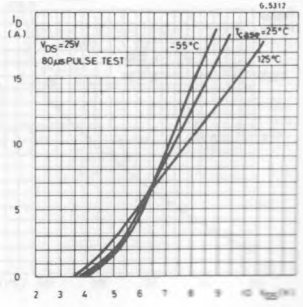
Output characteristics



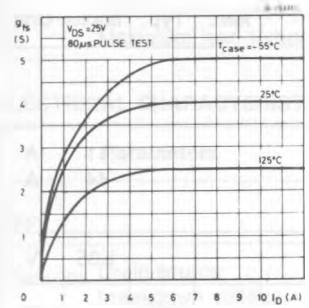
Output characteristics



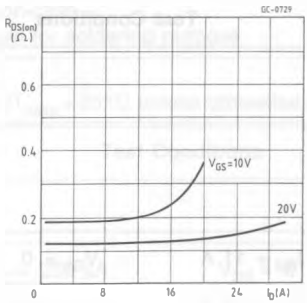
Transfer characteristics



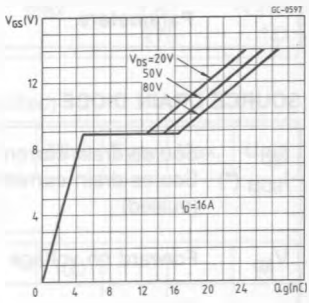
Transconductance



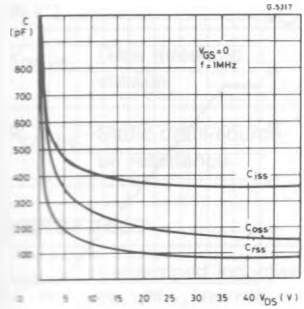
Static drain-source on resistance



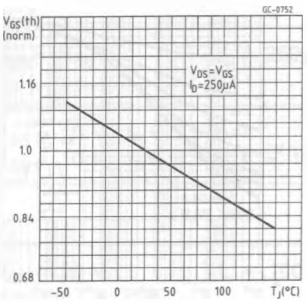
Gate charge vs gate-source voltage



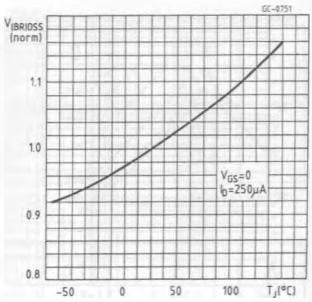
Capacitance variation



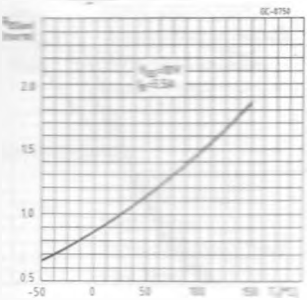
Normalized gate threshold voltage vs temperature



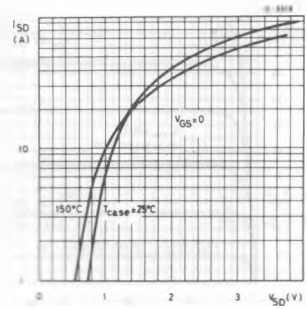
Normalized breakdown voltage vs temperature



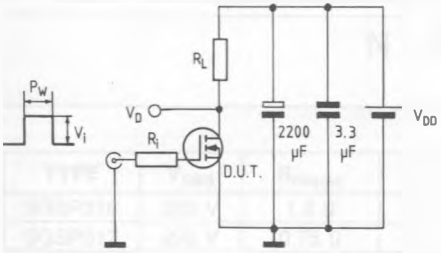
Normalized on resistance vs temperature



Source-drain diode forward characteristics

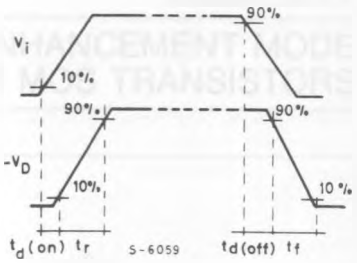


Switching times test circuit for resistive load

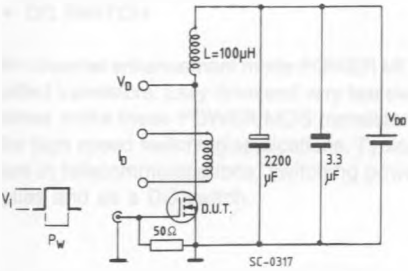


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

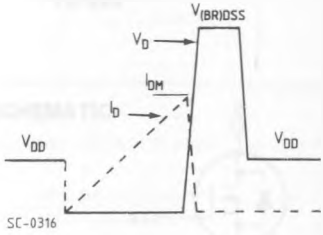


Unclamped inductive load test circuit

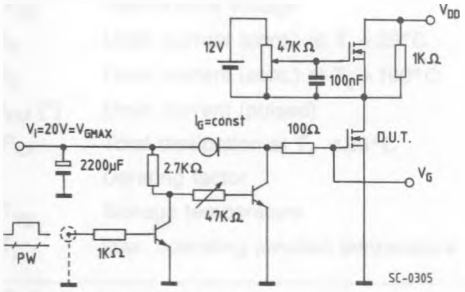


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit