

## N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

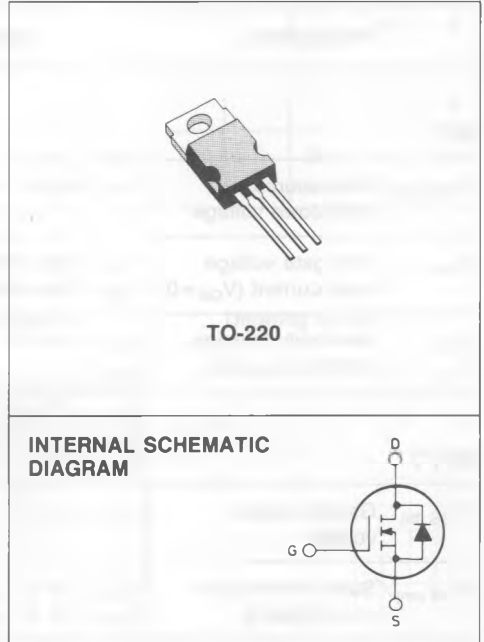
TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
SGSP330	450 V	3 Ω	3 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH VOLTAGE - 450V FOR OFF-LINE SMPS
- ULTRA FAST SWITCHING FOR OPERATION AT > 100KHz
- EASY DRIVE FOR REDUCED COST AND SIZE

**INDUSTRIAL APPLICATIONS:**

- SWITCHING POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include switching power supplies, uninterruptible power supplies and motor speed control.


**ABSOLUTE MAXIMUM RATINGS**

V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	450	V
V <sub>DGR</sub>	Drain-gate voltage (R <sub>GS</sub> = 20 KΩ)	450	V
V <sub>GS</sub>	Gate-source voltage	±20	V
I <sub>D</sub>	Drain current (cont.) at T <sub>c</sub> = 25°C	3	A
I <sub>D</sub>	Drain current (cont.) at T <sub>c</sub> = 100°C	1.9	A
I <sub>DM</sub> (*)	Drain current (pulsed)	12	A
I <sub>DLM</sub> (*)	Drain inductive current, clamped	12	A
P <sub>tot</sub>	Total dissipation at T <sub>c</sub> < 25°C	75	W
	Derating factor	0.6	W/°C
T <sub>stg</sub>	Storage temperature	-65 to 150	°C
T <sub>j</sub>	Max. operating junction temperature	150	°C

(\*) Pulse width limited by safe operating area

## THERMAL DATA

$R_{thj-case}$	Thermal resistance junction-case	max	1.67	°C/W
$T_L$	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS ( $T_{case} = 25^\circ\text{C}$  unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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## OFF

$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$	$V_{GS} = 0$	450			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$	$T_c = 125^\circ\text{C}$			250 1000	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 \text{ V}$				$\pm 100$	nA

## ON (\*)

$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ $V_{GS} = 10 \text{ V}$	$I_D = 1.5 \text{ A}$ $I_D = 1.5 \text{ A}$			3 6	$\Omega$ $\Omega$

## DYNAMIC

$g_{fs}$	Forward transconductance	$V_{DS} = 25 \text{ V}$	$I_D = 1.5 \text{ A}$	0.8			mho
$C_{iss}$	Input capacitance	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$	$f = 1 \text{ MHz}$		340	450	pF
$C_{oss}$	Output capacitance					95	pF
$C_{riss}$	Reverse transfer capacitance					50	pF

## SWITCHING

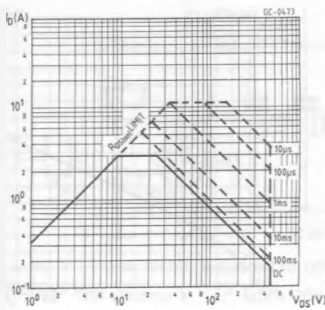
$t_{d(on)}$	Turn-on time	$V_{DD} = 225 \text{ V}$	$I_D = 1.5 \text{ A}$		10	15	ns
$t_r$	Rise time	$V_i = 10 \text{ V}$	$R_i = 4.7 \Omega$		25	35	ns
$t_{d(off)}$	Turn-off delay time	(see test circuit)			55	70	ns
$t_f$	Fall time				25	35	ns

ELECTRICAL CHARACTERISTICS (Continued)

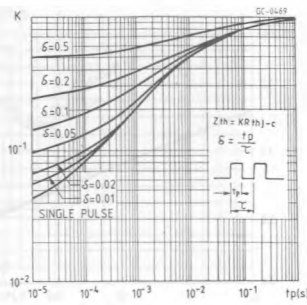
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}$ (*)	Source-drain current Source-drain current (pulsed)			3 12	A A
$V_{SD}$	Forward on voltage	$I_{SD} = 3\text{ A}$	$V_{GS} = 0$	1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 3\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$	$V_{GS} = 0$	360	ns

(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%  
 (\*) Pulse width limited by safe operating area

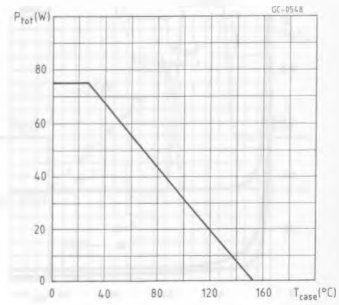
Safe operating areas



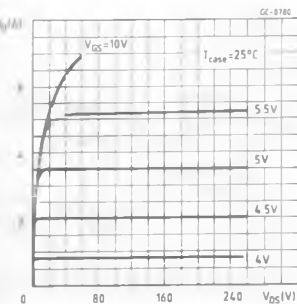
Thermal impedance



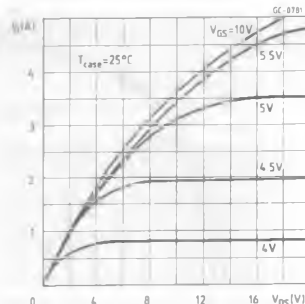
Derating curve



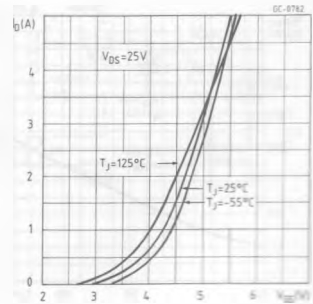
Output characteristics



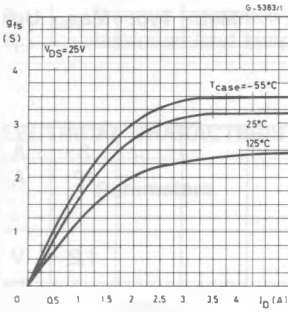
Output characteristics



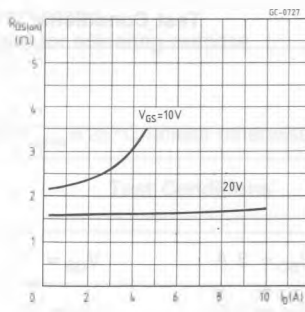
Transfer characteristics



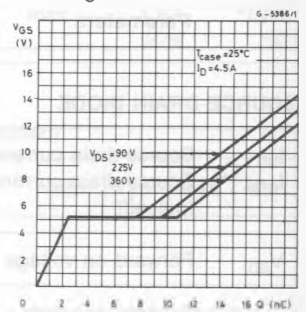
Transconductance



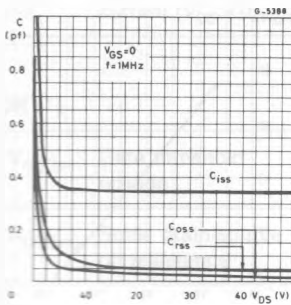
Static drain-source on resistance



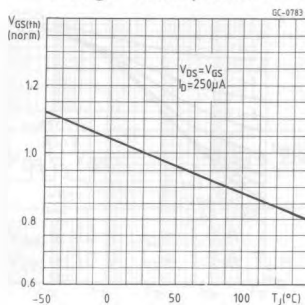
Gate charge vs gate-source voltage



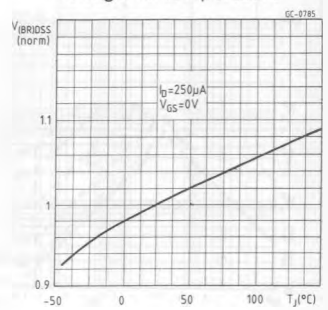
Capacitance variation



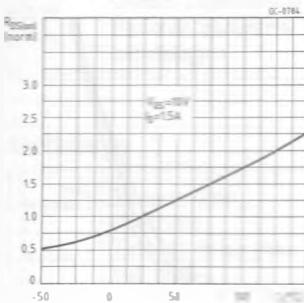
Normalized gate threshold voltage vs temperature



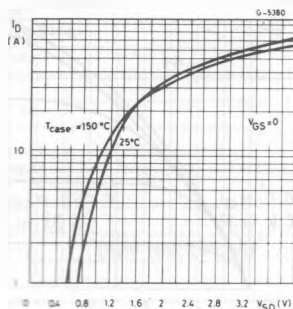
Normalized breakdown voltage vs temperature



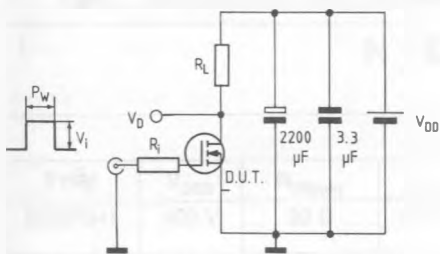
Normalized on resistance vs temperature



Source-drain diode forward characteristics

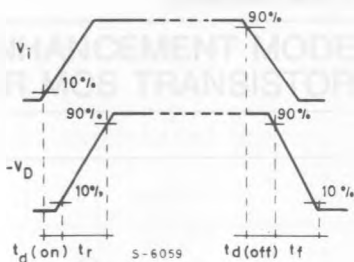


Switching times test circuit for resistive load

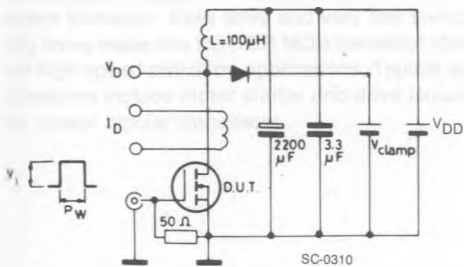


Pulse width  $\leq 100 \mu\text{s}$   
Duty cycle  $\leq 2\%$

Switching time waveforms for resistive load

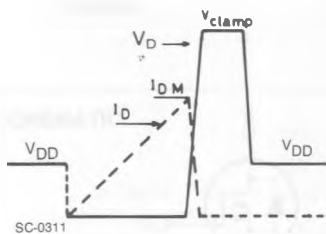


Clamped inductive load test circuit

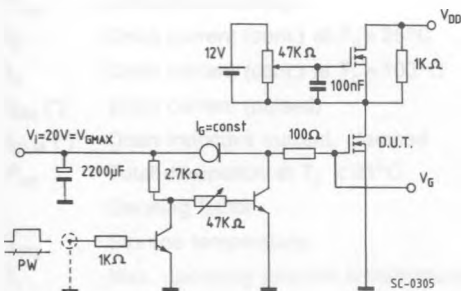


$V_i = 12 \text{ V}$  - Pulse width: adjusted to obtain specified  $I_{DM}$ ,  $V_{clamp} = 0.75 V_{(BR) DSS}$ .

Clamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required  $V_G$

Body-drain diode  $t_{rr}$  measurement  
Jedec test circuit

