SGS-THOMSON MICROELECTRONICS

SGSP491
SGSP492

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

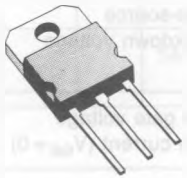
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP491	60 V	0.033 Ω	40 A
SGSP492	50 V	0.033 Ω	40 A

- HIGH SPEED SWITCHING APPLICATIONS
- 50 - 60 VOLTS FOR INVERTER AND UPS
- HIGH CURRENT - $V_{DS\ (on)} \leq 1V$ at 20A
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- EASY DRIVE - REDUCED SIZE AND COST

INDUSTRIAL APPLICATIONS:

- DC/DC CONVERTERS
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications such as DC/DC converters, UPS, inverters, battery changers and solar power converters.



TO-218

INTERNAL SCHEMATIC DIAGRAM

ABSOLUTE MAXIMUM RATINGS		SGSP491	SGSP492	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	60	50	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\ K\Omega$)	60	50	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c = 25°C$	40		A
I_D	Drain current (cont.) at $T_c = 100°C$	25		A
I_{DM} (*)	Drain current (pulsed)	160		A
P_{tot}	Total dissipation at $T_c < 25°C$	150		W
	Derating factor	1.2		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(*) Pulse width limited by safe operating area

◆ Introduced in 1988 week 44

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

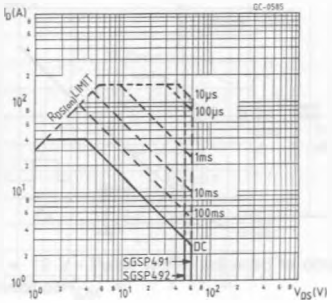
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP491** for **SGSP492**	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 20 A V_{GS} = 10 V I_D = 20 A T_c = 100°C			33 66	mΩ mΩ
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C	40			A
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 20 A	10			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	 V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1900	2800 1500 850	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 20 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		35 110 90 55	45 145 120 70	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

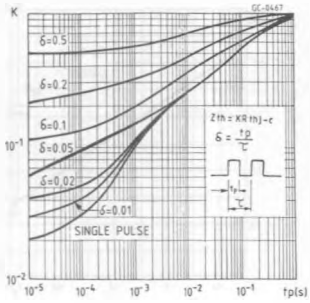
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)					40 160	A A
V_{SD}	Forward on voltage	I_{SD} = 40 A	V_{GS} = 0			1.4	V
t_{rr}	Reverse recovery time	I_{SD} = 40 A di/dt = 25 A/μs	V_{GS} = 0		140		ns

(•) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

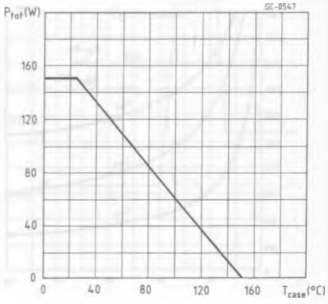
Safe operating areas



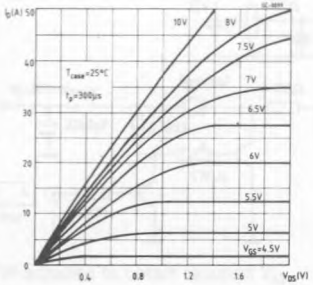
Thermal impedance



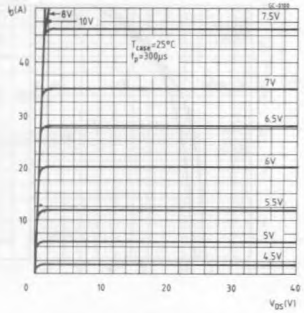
Derating curve



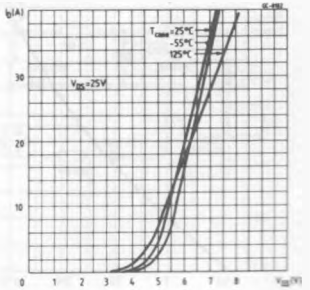
Output characteristics



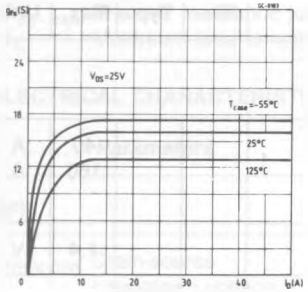
Output characteristics



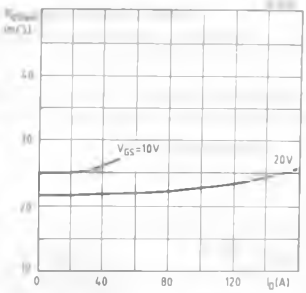
Transfer characteristics



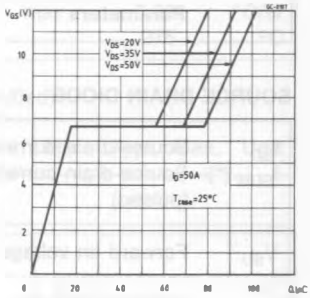
Transconductance



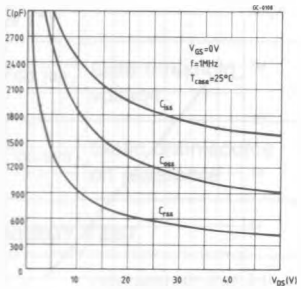
Static drain-source on resistance



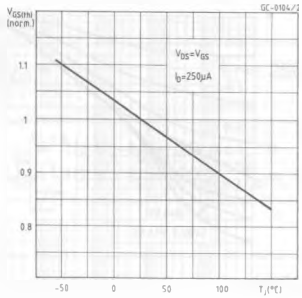
Gate charge vs gate-source voltage



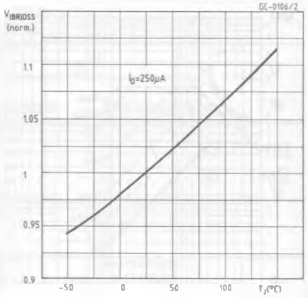
Capacitance variation



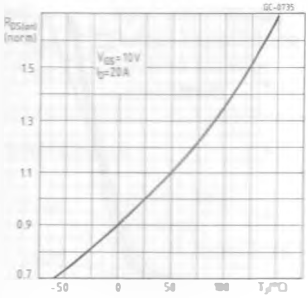
Normalized gate threshold voltage vs temperature



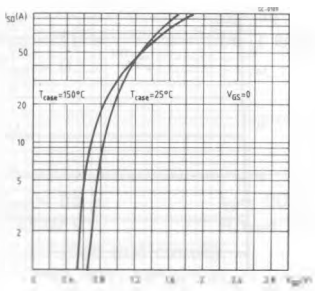
Normalized breakdown voltage vs temperature



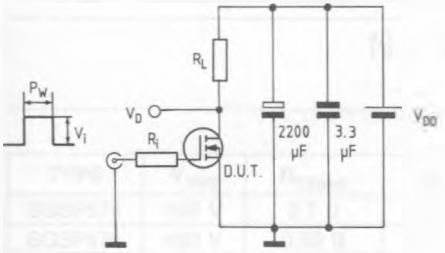
Normalized on resistance vs temperature



Source-drain diode forward characteristics

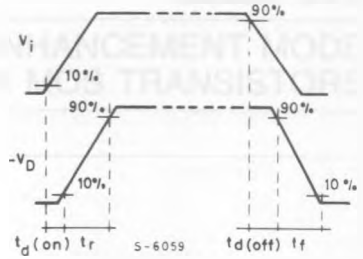


Switching times test circuit for resistive load

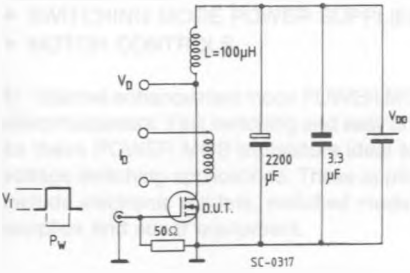


Pulse width ≤ 100 µs
Duty cycle ≤ 2%

Switching time waveforms for resistive load

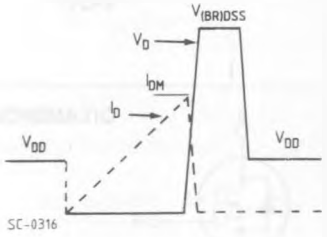


Unclamped inductive load test circuit

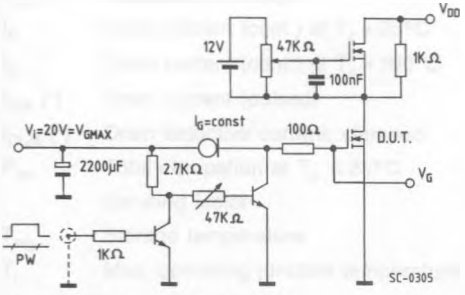


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit