

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

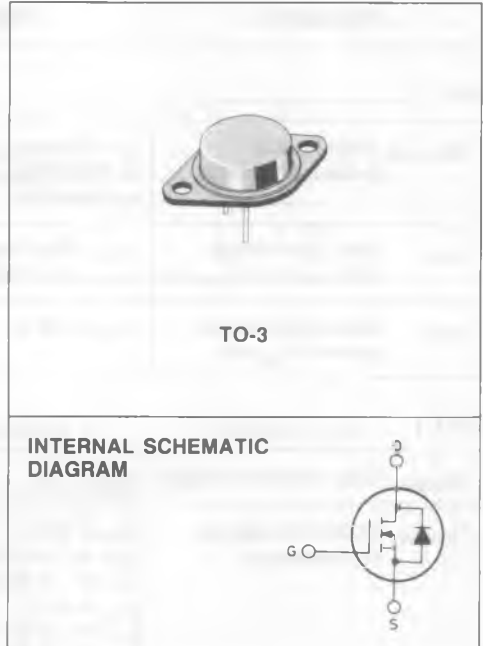
TYPE	V _{DSS}	R _{DS(on)}	I _D
SGSP574	450 V	0.7 Ω	9 A
SGSP575	400 V	0.55 Ω	10 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH VOLTAGE - FOR OFF-LINE SMPS
- HIGH CURRENT - FOR SMPS UP TO 350W
- ULTRA FAST SWITCHING - FOR OPERATION AT > 100kHz
- EASY DRIVE FOR REDUCED SIZE AND COST

INDUSTRIAL APPLICATIONS:

- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Fast switching and easy drive make these POWER MOS transistors ideal for high voltage switching applications. These applications include electronic welders, switched mode power supplies and sonar equipment.



ABSOLUTE MAXIMUM RATINGS

	SGSP574	SGSP575	
V _{DS}	450	400	V
V _{DGR}	450	400	V
V _{GS}		± 20	V
I _D	9	10	A
I _D	5.6	6.3	A
I _{DM} (*)	40	40	A
I _{DLM} (*)	40	40	A
P _{tot}		150	W
		1.2	W/°C
T _{stg}	-65 to 150		°C
T _j	150		°C

(*) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj - case}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^\circ\text{C}$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR) DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ for SGSP574 for SGSP575	$V_{GS} = 0$	450 400		V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$	$T_c = 125^\circ\text{C}$		250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 100	nA

ON (*)

$V_{GS (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu\text{A}$	2		4	V
$R_{DS (on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ $I_D = 4.5 \text{ A}$ for SGSP574 $I_D = 5 \text{ A}$ for SGSP575 $V_{GS} = 10 \text{ V}$ $T_c = 100^\circ\text{C}$ $I_D = 4.5 \text{ A}$ for SGSP574 $I_D = 5 \text{ A}$ for SGSP575				0.7 0.55 1.4 1.1	Ω Ω Ω Ω

DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} = 25 \text{ V}$	$I_D = 5 \text{ A}$	6			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$	$f = 1 \text{ MHz}$		1600	2100 390 260	pF pF pF

SWITCHING

$t_d (on)$	Turn-on time	$V_{DD} = 225 \text{ V}$	$I_D = 5 \text{ A}$		30	40	ns
t_r	Rise time	$V_i = 10 \text{ V}$	$R_i = 4.7 \Omega$		45	60	ns
$t_d (off)$	Turn-off delay time	(see test circuit)			125	165	ns
t_f	Fall time				30	40	ns

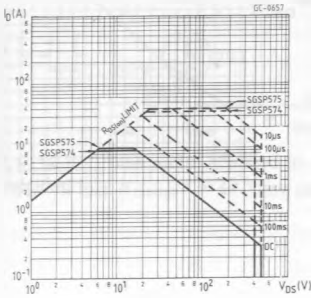
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current	for SGSP574 for SGSP575			9 10 40	A A A
$I_{SDM} (*)$	Source-drain current (pulsed)					
V_{SD}	Forward on voltage	$V_{GS} = 0$ $I_{SD} = 9\text{ A}$ for SGSP574 $I_{SD} = 10\text{ A}$ for SGSP575			1.2 1.2	V V
t_{rr}	Reverse recovery time	$I_{SD} = 10\text{ A}$ $V_{GS} = 0$ $di/dt = 100\text{ A}/\mu\text{s}$		420		ns

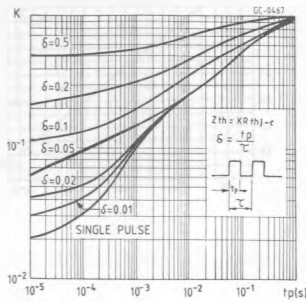
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

(*) Pulse width limited by safe operating area

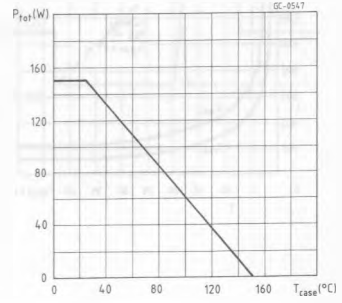
Safe operating areas



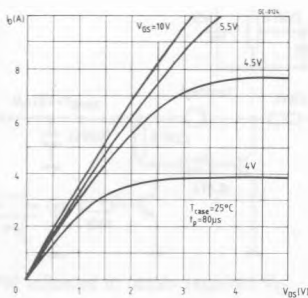
Thermal impedance



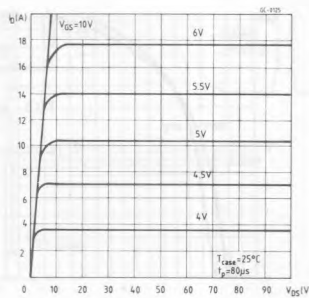
Derating curve



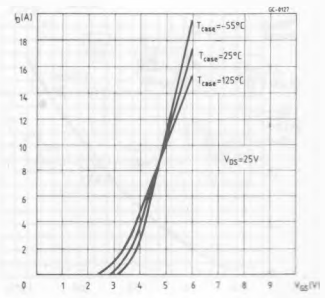
Output characteristics



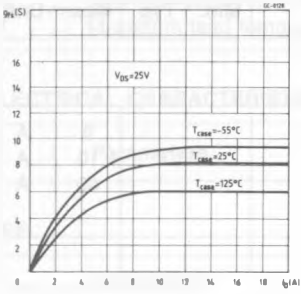
Output characteristics



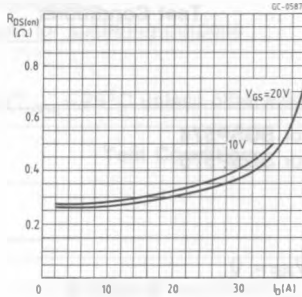
Transfer characteristics



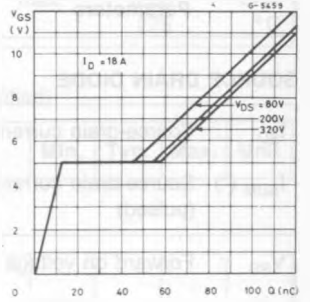
Transconductance



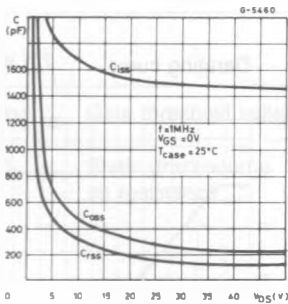
Static drain-source on resistance



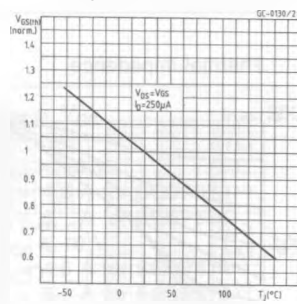
Gate charge vs gate-source voltage



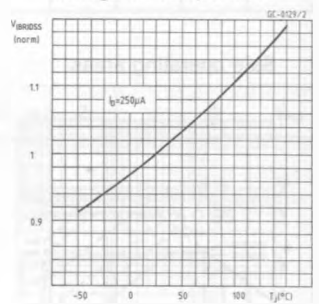
Capacitance variation



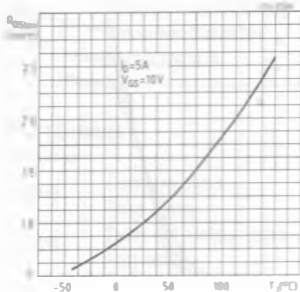
Normalized gate threshold voltage vs temperature



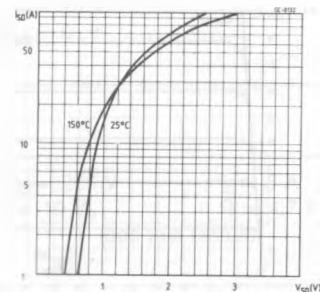
Normalized breakdown voltage vs temperature



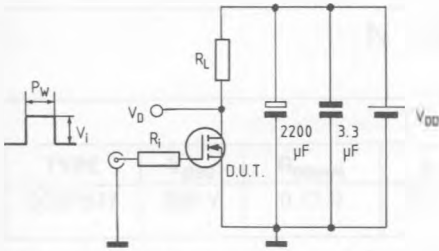
Normalized on resistance vs temperature



Source-drain diode forward characteristics



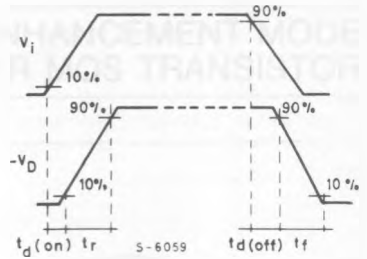
Switching times test circuit for resistive load



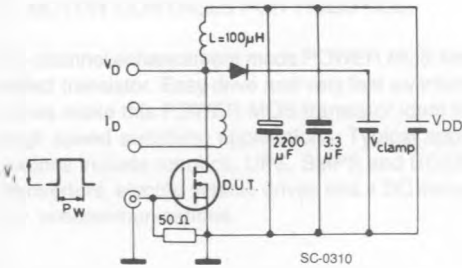
Pulse width $\leq 100 \mu\text{s}$
 Duty cycle $\leq 2\%$

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Switching time waveforms for resistive load



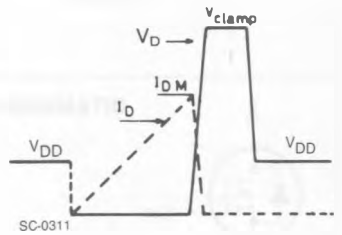
Clamped inductive load test circuit



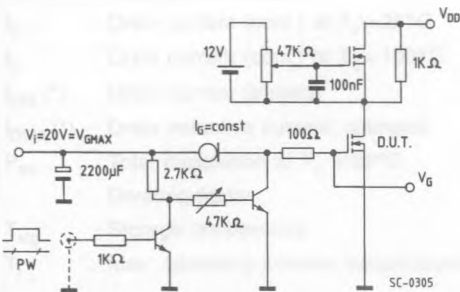
$V_i = 12 \text{ V}$ - Pulse width: adjusted to obtain specified I_{DM} . $V_{clamp} = 0.75 V_{(BR)}$ DSS.

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Clamped inductive waveforms



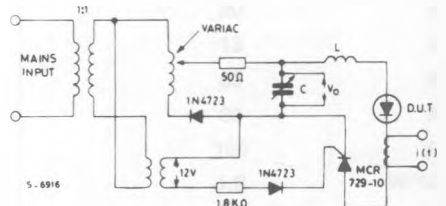
Gate charge test circuit



PW adjusted to obtain required V_G

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Body-drain diode t_{rr} measurement
 Jedec test circuit



S-6016