

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

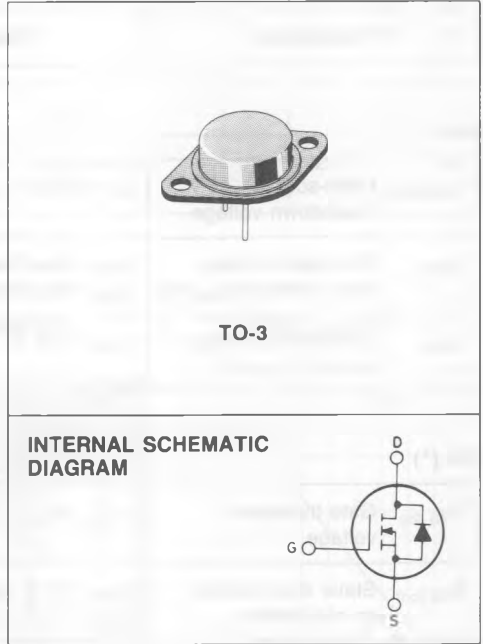
TYPE	V _{DSS}	R _{DS(on)}	I _D
SGSP579	500 V	0.7 Ω	9 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH VOLTAGE - 9A FOR UP TO 350W SMPS
- ULTRA FAST SWITCHING - FOR OPERATION AT > 100KHz
- EASY DRIVE - REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include switching mode power supplies, uninterruptible power supplies and motor speed control.


ABSOLUTE MAXIMUM RATINGS

V _{DS}	Drain-source voltage (V _{GS} = 0)	500	V
V _{DGR}	Drain-gate voltage (R _{GS} = 20 KΩ)	500	V
V _{GS}	Gate-source voltage	±20	V
I _D	Drain current (cont.) at T _c = 25°C	9	A
I _D	Drain current (cont.) at T _c = 100°C	5.6	A
I _{DM} (*)	Drain current (pulsed)	36	A
I _{DLM} (*)	Drain inductive current, clamped	36	A
P _{tot}	Total dissipation at T _c < 25°C	150	W
	Derating factor	1.2	W/°C
T _{stg}	Storage temperature	-65 to 150	°C
T _j	Max. operating junction temperature	150	°C

(*) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj-case}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^\circ\text{C}$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$	$V_{GS} = 0$	500		V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$			250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 100	nA

ON (*)

$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ $I_D = 4.5 \text{ A}$ $V_{GS} = 10 \text{ V}$ $I_D = 4.5 \text{ A}$ $T_c = 100^\circ\text{C}$				0.7 1.4	Ω Ω

DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} = 25 \text{ V}$	$I_D = 4.5 \text{ A}$	5			mho	
C_{iss}	Input capacitance	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$	$f = 1 \text{ MHz}$		1600	1900	pF	
C_{oss}	Output capacitance					280		pF
C_{rss}	Reverse transfer capacitance						170	

SWITCHING

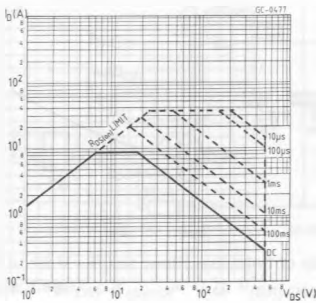
$t_{d(on)}$	Turn-on time	$V_{DD} = 250 \text{ V}$ $V_i = 10 \text{ V}$	$I_D = 4.5 \text{ A}$ $R_i = 4.7 \Omega$		30	40	ns
t_r	Rise time				40	60	ns
$t_{d(off)}$	Turn-off delay time	(see test circuit)			130	170	ns
t_f	Fall time				30	40	ns

ELECTRICAL CHARACTERISTICS (Continued)

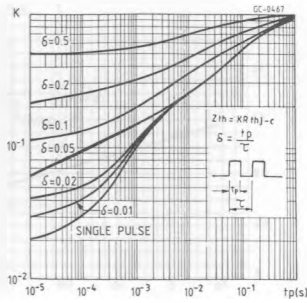
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} Source-drain current $I_{SDM} (*)$ Source-drain current (pulsed)				9 36	A A
V_{SD} Forward on voltage	$I_{SD} = 9\text{ A}$ $V_{GS} = 0$			1.15	V
t_{rr} Reverse recovery time	$I_{SD} = 9\text{ A}$ $V_{GS} = 0$ $di/dt = 100\text{ A}/\mu\text{s}$		420		ns

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5%
 (*) Pulse width limited by safe operating area

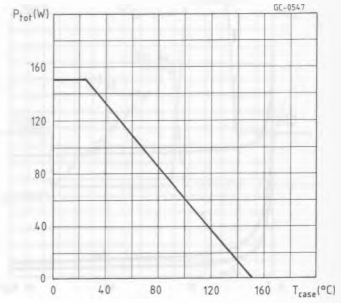
Safe operating areas



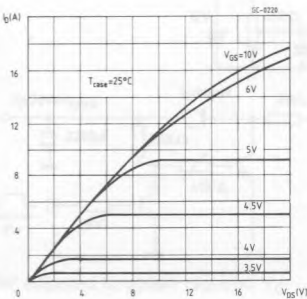
Thermal impedance



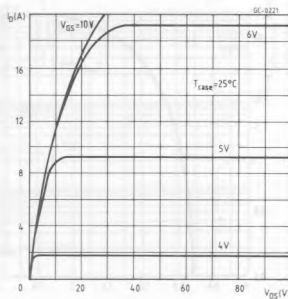
Derating curve



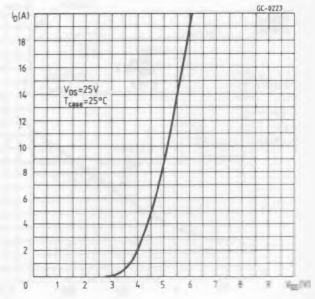
Output characteristics



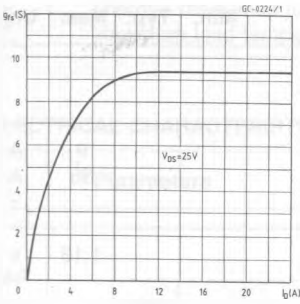
Output characteristics



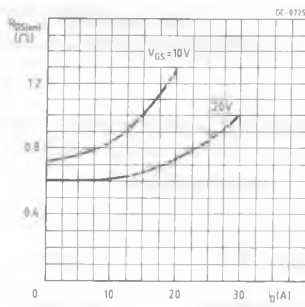
Transfer characteristics



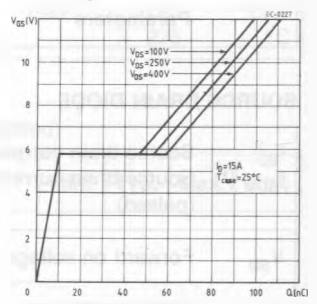
Transconductance



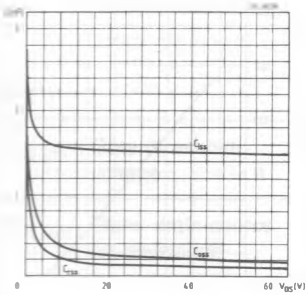
Static drain-source on resistance



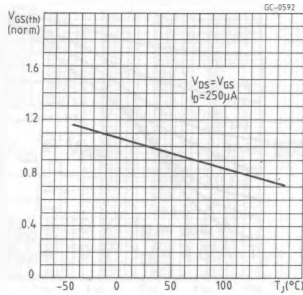
Gate charge vs gate-source voltage



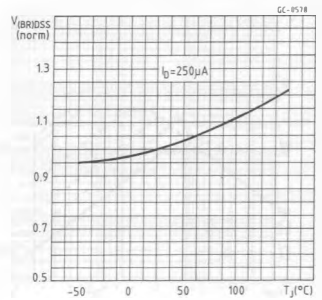
Capacitance variation



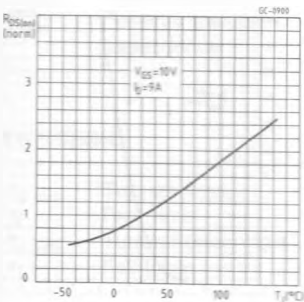
Normalized gate threshold voltage vs temperature



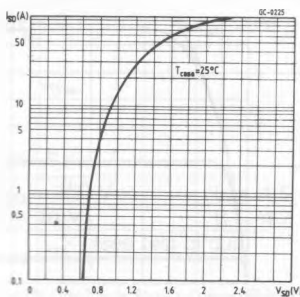
Normalized breakdown voltage vs temperature



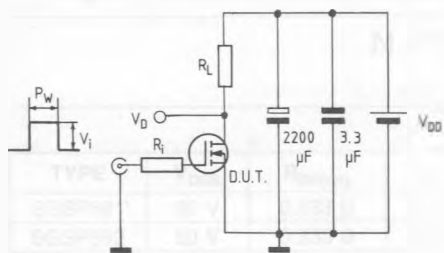
Normalized on resistance vs temperature



Source-drain diode forward characteristics



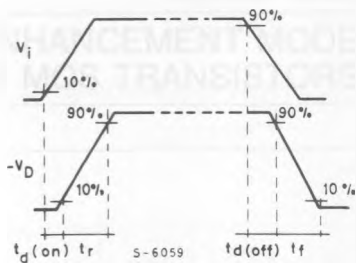
Switching times test circuit for resistive load



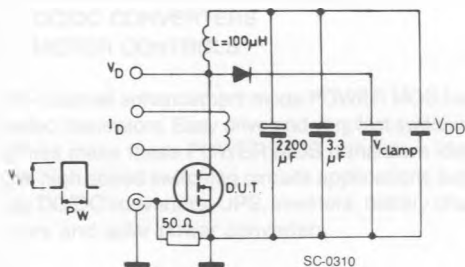
Pulse width $\leq 100 \mu\text{s}$
 Duty cycle $\leq 2\%$

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Switching time waveforms for resistive load

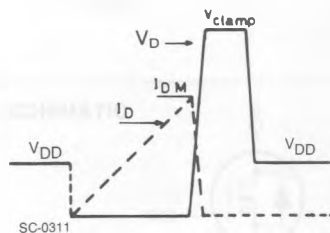


Clamped inductive load test circuit

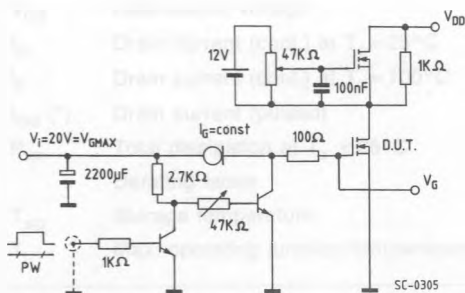


$V_i = 12 \text{ V}$ - Pulse width: adjusted to obtain specified I_{DM} . $V_{\text{clamp}} = 0.75 V_{(BR) \text{ DSS}}$

Clamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
 Jedec test circuit

