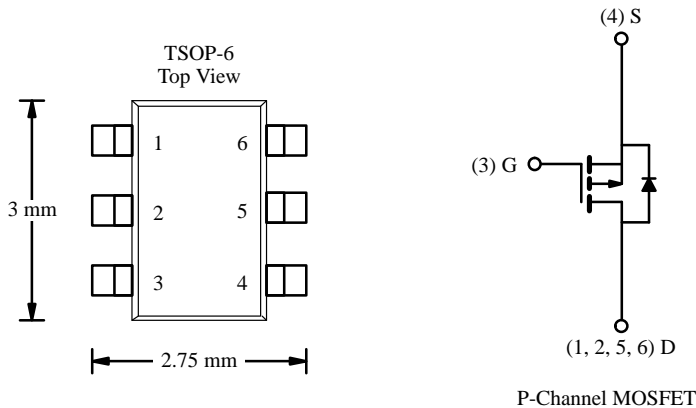


P-Channel Enhancement-Mode MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
-30	0.100 @ V _{GS} = -10 V	±3.5
	0.190 @ V _{GS} = -4.5 V	±2.5

TrenchFET™
Power MOSFETs



Power Dissipation
Si3455DV—2.0 W

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	-30	V	
Gate-Source Voltage	V _{GS}	±20		
Continuous Drain Current (T _J = 150°C) ^{NO TAG}	I _D	T _A = 25°C	±3.5	A
		T _A = 70°C	±2.7	
Pulsed Drain Current	I _{DM}	±20		
Continuous Source Current (Diode Conduction) ^{NO TAG}	I _S	-1.7		
Maximum Power Dissipation ^{NO TAG}	P _D	T _A = 25°C	2.0	W
		T _A = 70°C	1.3	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C	

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^{NO TAG}	R _{thJA}	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 5 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1255.

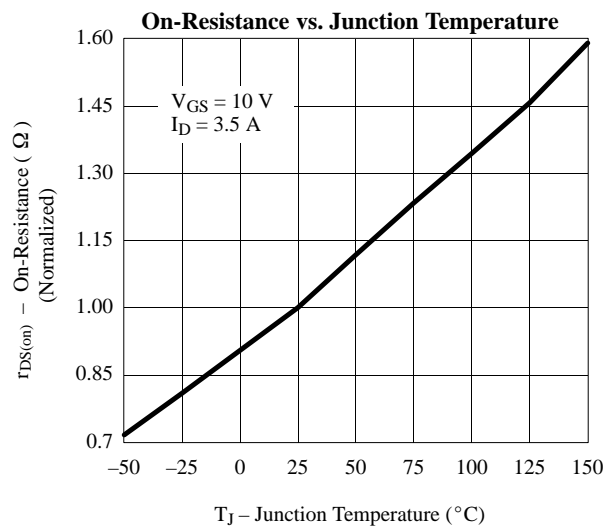
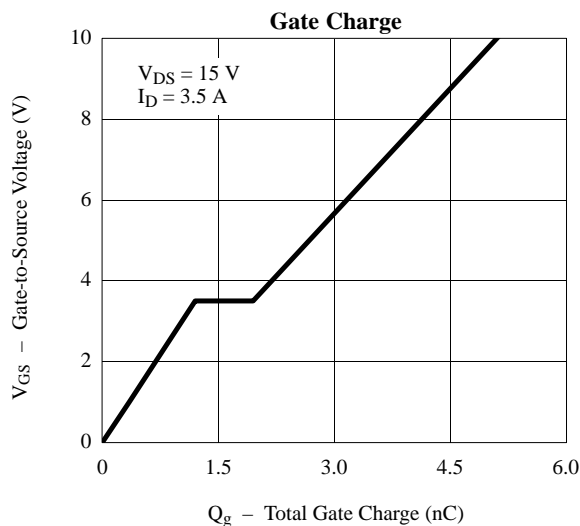
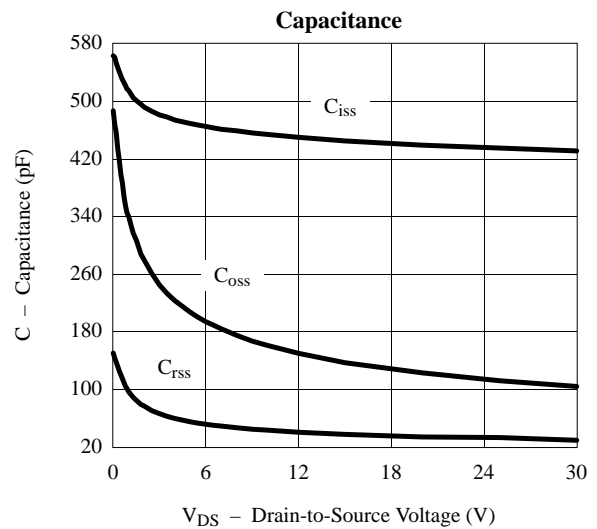
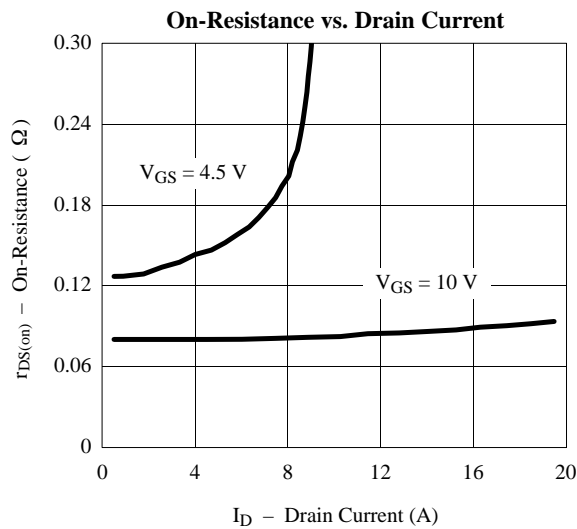
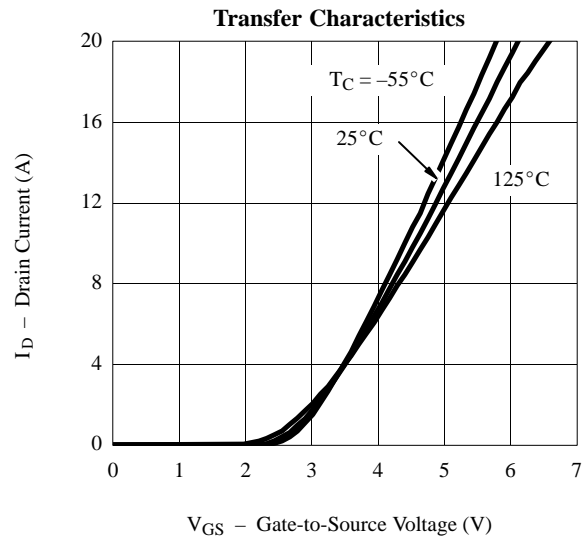
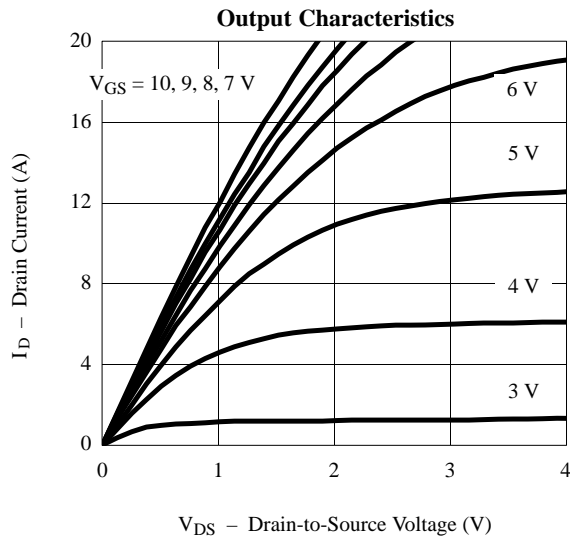
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	-1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			-5	
On-State Drain Current ^{NO TAG}	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -10\ \text{V}$	-15			A
Drain-Source On-State Resistance ^{NO TAG}	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = 3.5\ \text{A}$		0.080	0.100	Ω
		$V_{GS} = -4.5\ \text{V}, I_D = 2.5\ \text{A}$		0.134	0.190	
Forward Transconductance ^{NO TAG}	g_{fs}	$V_{DS} = -15\ \text{V}, I_D = -3.5\ \text{A}$		4.0		S
Diode Forward Voltage ^{NO TAG}	V_{SD}	$I_S = -1.7\ \text{A}, V_{GS} = 0\ \text{V}$			-1.2	V
Dynamic^{NO TAG}						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -3.5\ \text{A}$		5.1	10	nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			1.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -10\ \text{V}, R_G = 6\ \Omega$		10	20	ns
Rise Time	t_r			15	30	
Turn-Off Delay Time	$t_{d(off)}$			20	35	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		50	80	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

