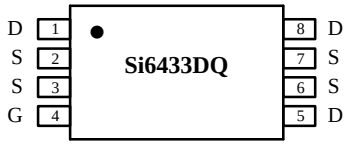
P-Channel Enhancement-Mode MOSFET

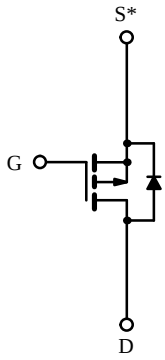
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–12	0.06 @ V_{GS} = –4.5 V	± 4.0
	0.09 @ V_{GS} = –2.5 V	± 3.0

TSSOP-8



Top View



*Source Pins 2, 3, 6 and 7 must be tied common.

P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–12	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 4.0	A
	T_A = 70°C		± 3.2	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction)[a]		I_S	–1.4	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.5	W
	T_A = 70°C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	83	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1801. A SPICE Model data sheet is available for this product (FaxBack document #5122).

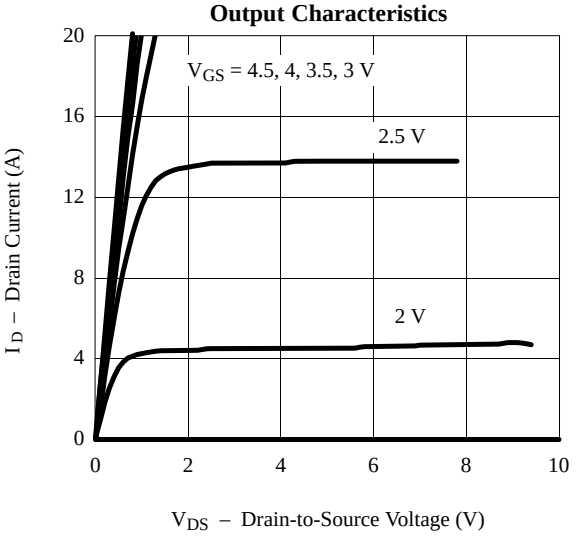
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	–0.6			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –12 V, V_{GS} = 0 V			–1	µA
		V_{DS} = –12 V, V_{GS} = 0 V, T_J = 70°C			–25	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = –5 V, V_{GS} = –4.5 V	–10			A
		V_{DS} = –5 V, V_{GS} = –2.5 V	–4			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = –4.5 V, I_D = 4.0 A		0.040	0.06	Ω
		V_{GS} = –2.5 V, I_D = 2.0 A		0.060	0.09	
Forward Transconductance[a]	g_{fs}	V_{DS} = –9 V, I_D = –4.0 A		13		S
Diode Forward Voltage[a]	V_{SD}	I_S = –1.4 A, V_{GS} = 0 V		–0.8	–1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –4.0 A		20	40	nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			6.0		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –6 V, R_L = 6 Ω I_D ≅ –1 A, V_{GEN} = –4.5 V, R_G = 6 Ω		26	60	ns
Rise Time	t_r			47	100	
Turn-Off Delay Time	$t_{d(off)}$			87	180	
Fall Time	t_f			47	100	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = –1.4 A, di/dt = 100 A/µs		70	100	

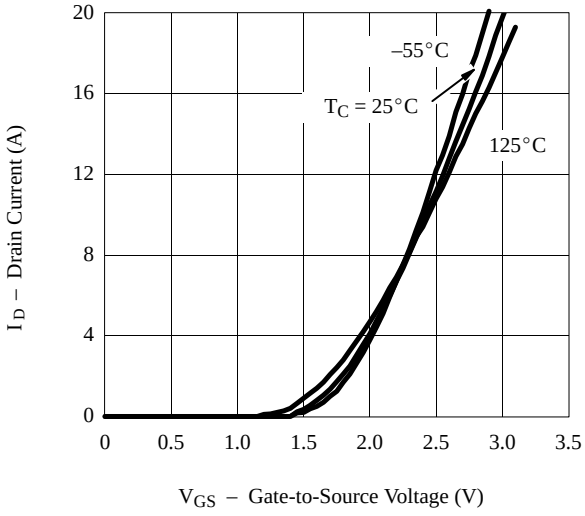
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)

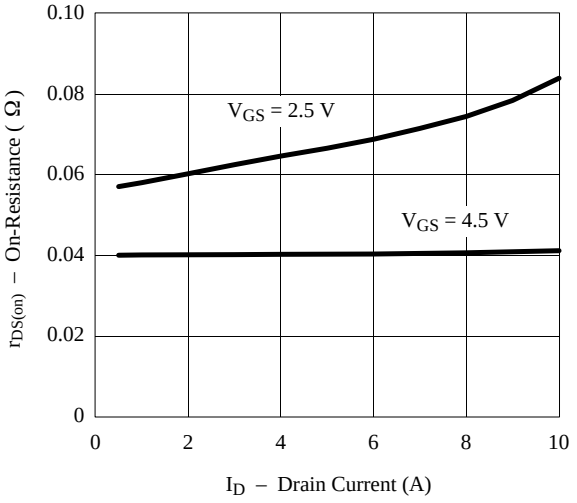
Output Characteristics



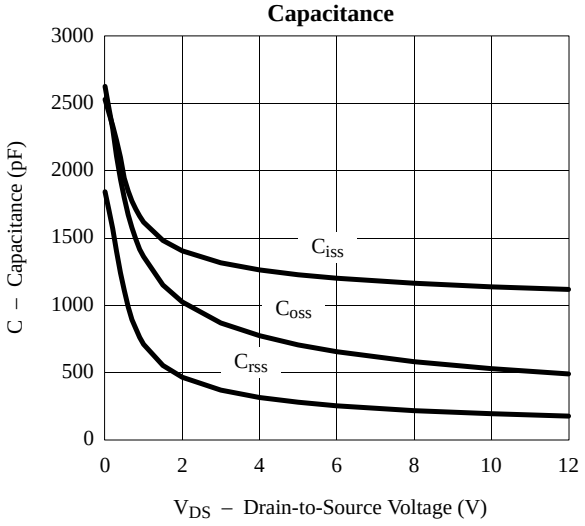
Transfer Characteristics



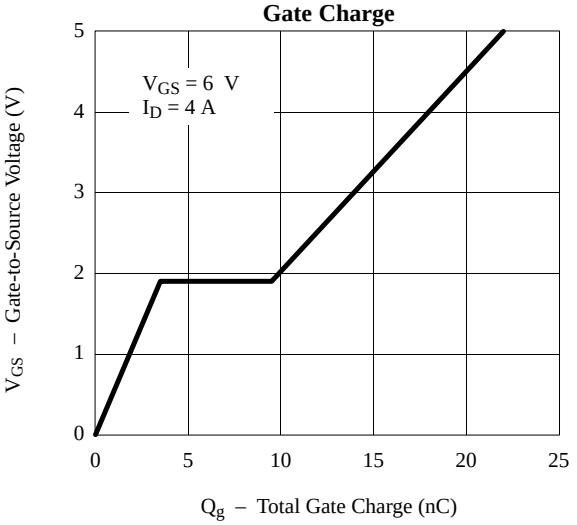
On-Resistance vs. Drain Current



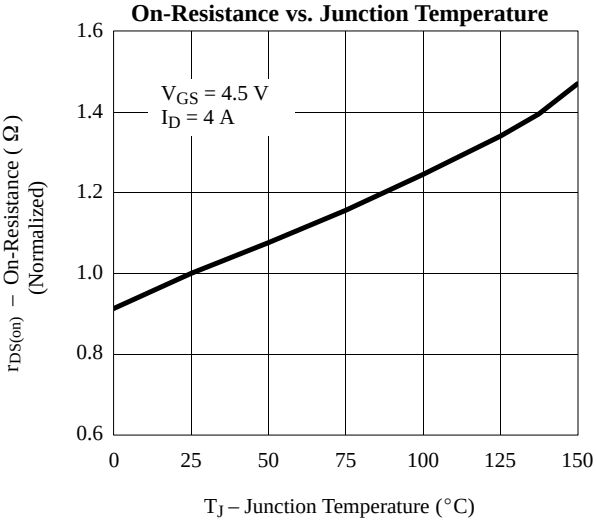
Capacitance



Gate Charge

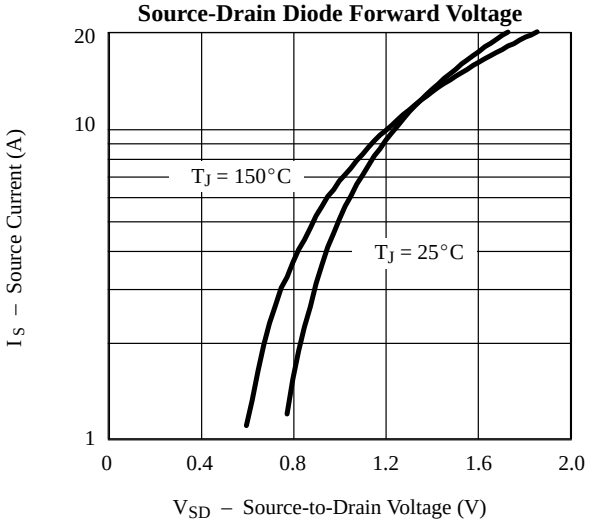


On-Resistance vs. Junction Temperature

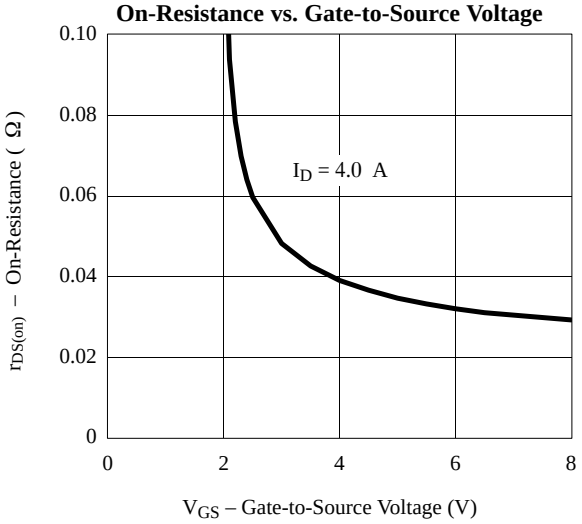


Typical Characteristics (25°C Unless Noted)

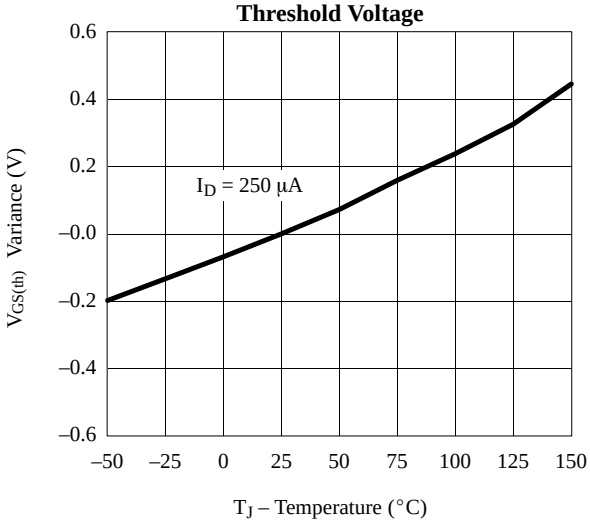
Source-Drain Diode Forward Voltage



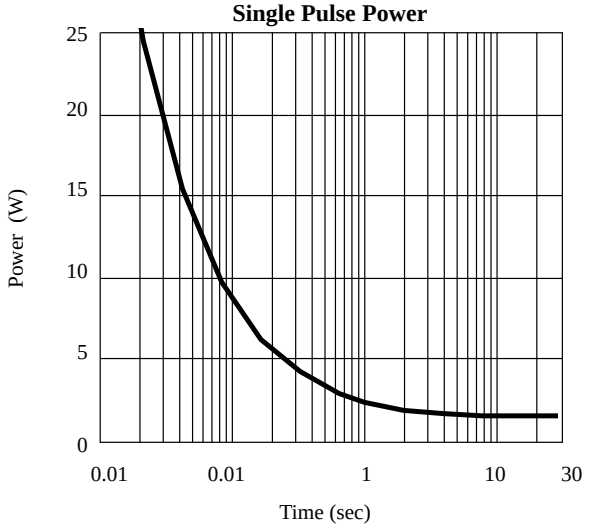
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient