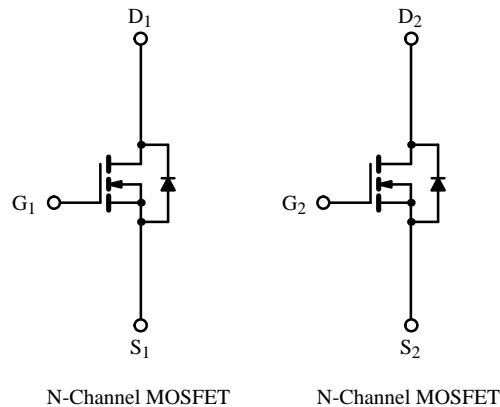
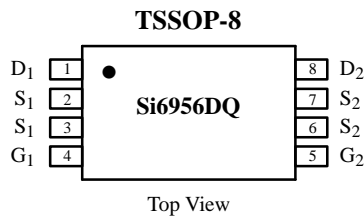


Dual N-Channel Enhancement-Mode MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
20	0.09 @ V _{GS} = 10 V	± 2.5
	0.175 @ V _{GS} = 4.5 V	± 1.8



Absolute Maximum Ratings (T_A = 25 °C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	± 2.5
		T _A = 70 °C	± 2.0
Pulsed Drain Current	I _{DM}	± 20	A
Continuous Source Current (Diode Conduction) ^a	I _S	1.25	
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	1.0
		T _A = 70 °C	0.64
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	125	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1807. A SPICE Model data sheet is available for this product (FaxBack document #5125).

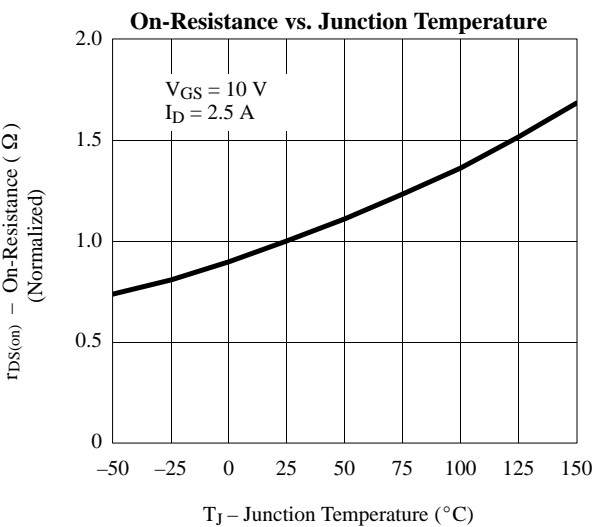
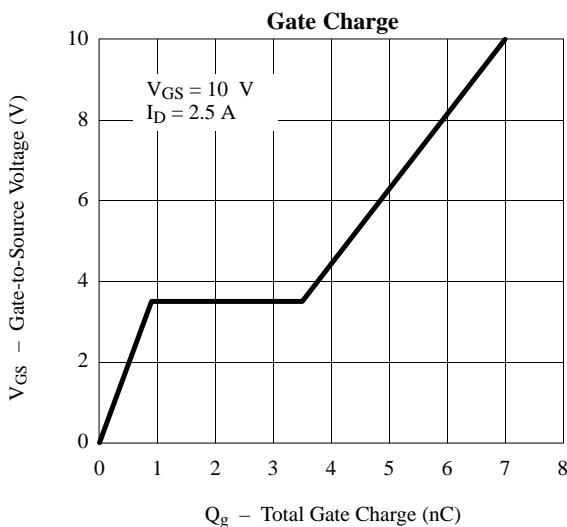
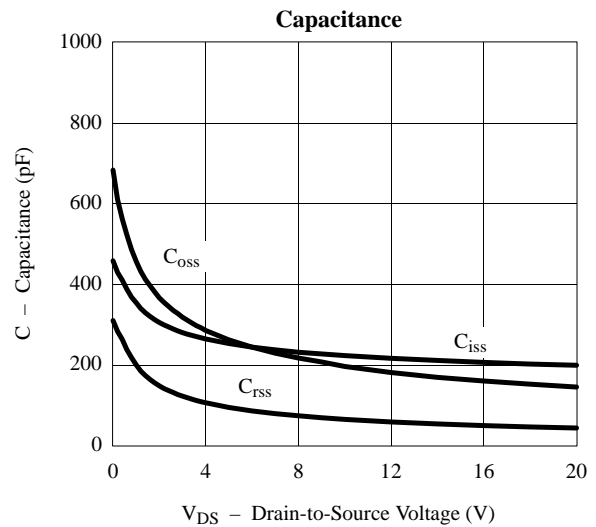
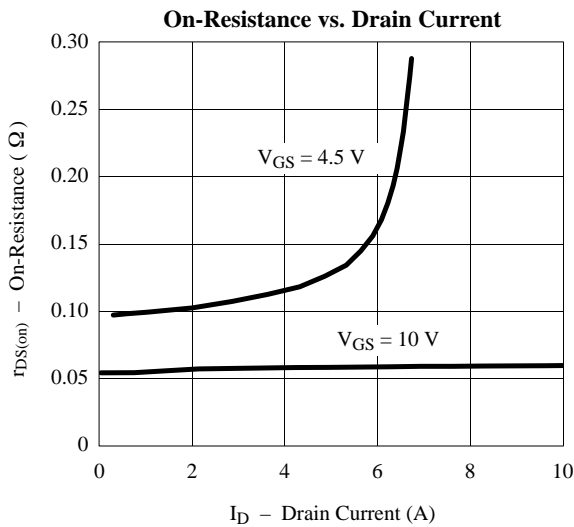
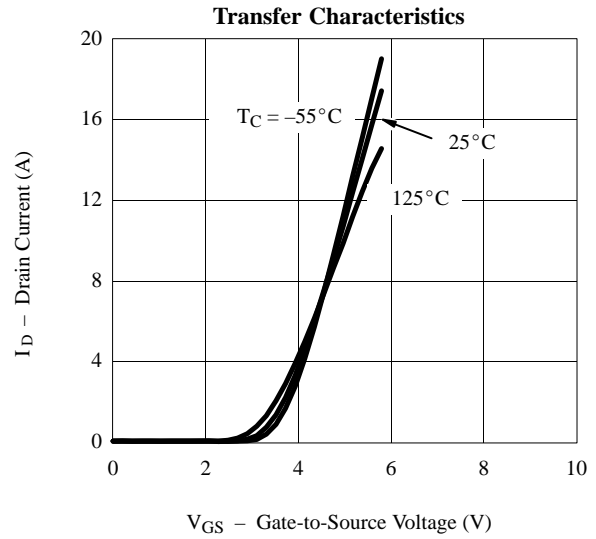
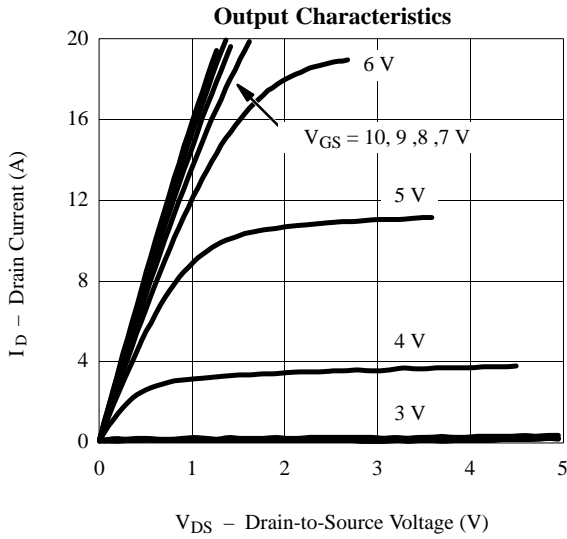
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	14			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 2.5 \text{ A}$		0.065	0.09	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 1.8 \text{ A}$		0.100	0.175	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 2.5 \text{ A}$		5		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.25 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 2.5 \text{ A}$		7	10	nC
Gate-Source Charge	Q_{gs}			0.9		
Gate-Drain Charge	Q_{gd}			2.1		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10 \text{ V}, R_L = 10 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$		11	20	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			16	30	
Fall Time	t_f			6	15	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		45	70	

Notes

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

