

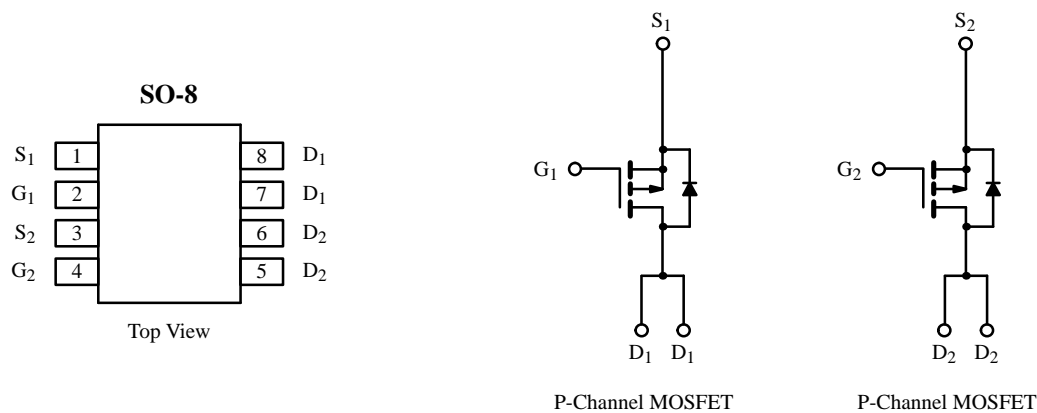
Dual P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.11 @ $V_{GS} = -4.5$ V	± 3.4
	0.15 @ $V_{GS} = -3.0$ V	± 2.9
	0.19 @ $V_{GS} = -2.7$ V	± 2.6

Recommended upgrade: Si9934DY

Lower profile/smaller size—see LITE FOOT® equivalent: Si6943DQ



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	± 3.4
		$T_A = 70^\circ\text{C}$	± 2.7
Pulsed Drain Current	I_{DM}	± 8	A
Continuous Source Current (Diode Conduction) ^a	I_S	-2.0	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.0
		$T_A = 70^\circ\text{C}$	1.3
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C}/\text{W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1209. A SPICE Model data sheet is available for this product (FaxBack document #5121).

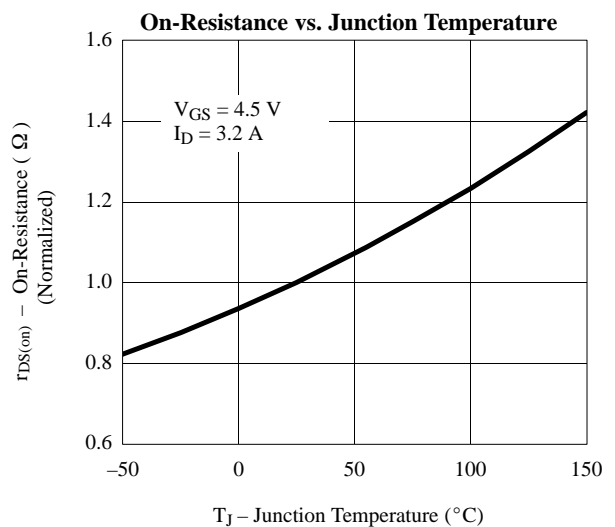
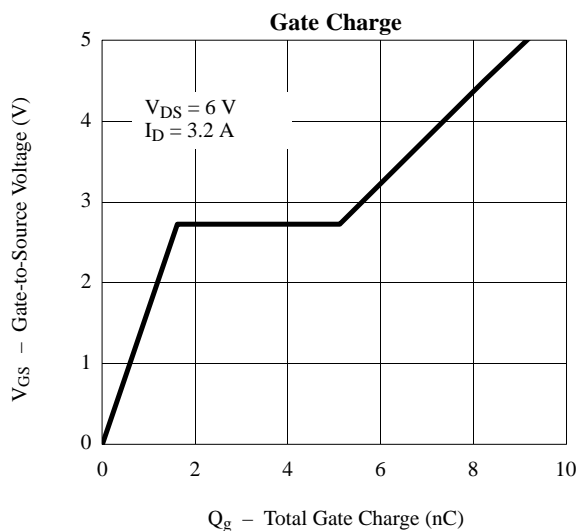
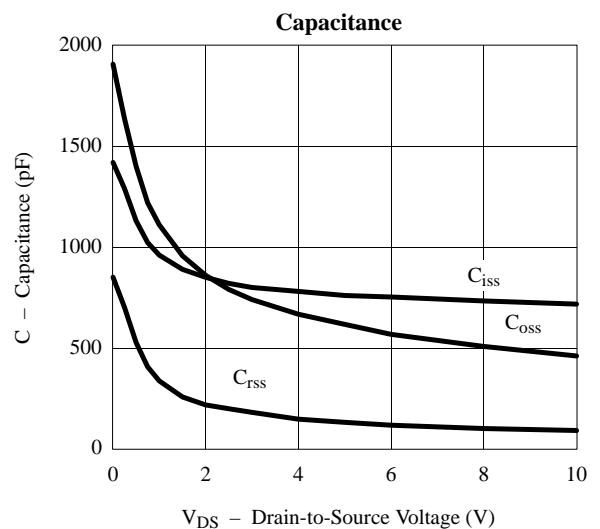
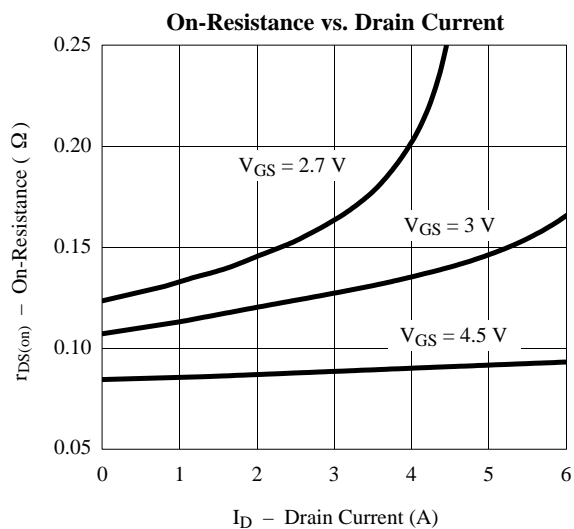
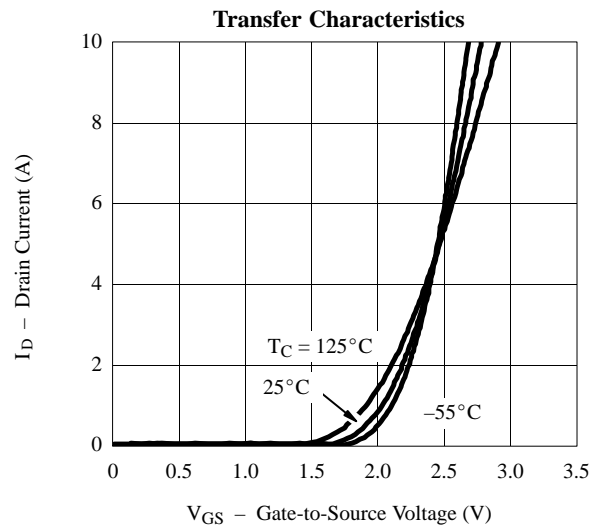
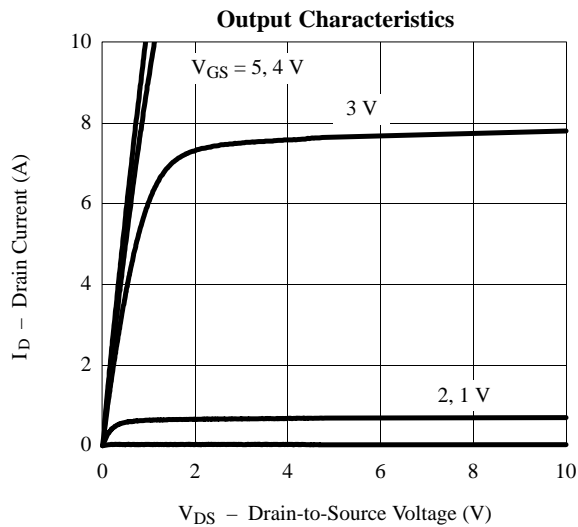
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.8			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -10\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 85^\circ\text{C}$			-3	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-8			A
		$V_{DS} \leq -5\ \text{V}, V_{GS} = -2.7\ \text{V}$	-2			
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = -3.2\ \text{A}$		0.09	0.11	Ω
		$V_{GS} = -3.0\ \text{V}, I_D = -2.0\ \text{A}$		0.120	0.15	
		$V_{GS} = -2.7\ \text{V}, I_D = -1\ \text{A}$		0.135	0.19	
Forward Transconductance ^b	g_{fs}	$V_{DS} = -9\ \text{V}, I_D = -3.4\ \text{A}$		8		S
Diode Forward Voltage ^b	V_{SD}	$I_S = -2.0\ \text{A}, V_{GS} = 0\ \text{V}$		-0.9	-1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = -6\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -3.2\ \text{A}$		8	20	nC
Gate-Source Charge	Q_{gs}			1.6		
Gate-Drain Charge	Q_{gd}			3.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\ \text{V}, R_L = 6\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_G = 6\ \Omega$		22	40	ns
Rise Time	t_r			43	80	
Turn-Off Delay Time	$t_{d(off)}$			35	70	
Fall Time	t_f			20	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.0\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		75	100	

Notes

- a. For design aid only; not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



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