SGS-THOMSON MICROELECTRONICS

STLT20
STLT19

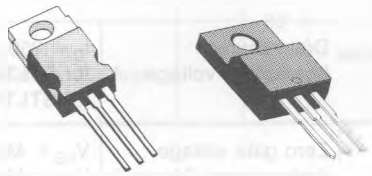
N - CHANNEL ENHANCEMENT MODE LOW THRESHOLD POWER MOS TRANSISTORS

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STLT20	60 V	0.15 Ω	15 A
STLT20FI	60 V	0.15 Ω	10 A
STLT19	50 V	0.15 Ω	15 A
STLT19FI	50 V	0.15 Ω	10 A

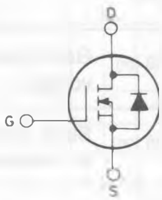
- LOGIC LEVEL (+5V) CMOS/TTL COMPATIBLE INPUT
- HIGH INPUT IMPEDANCE
- ULTRA FAST SWITCHING

N - channel enhancement mode POWER MOS field effect transistors. The low input voltage - logic level - and easy drive make these devices ideal for automotive and industrial applications. Typical uses are in relay and actuator driving in the automotive enviroment.



TO-220 ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		STLT20 / STLT20FI	STLT19 / STLT19FI	
	TO-220 ISOWATT220			
V_{DS}	Drain-source voltage ($V_{GS}=0$)	60	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	60	50	V
V_{GS}	Gate-source voltage	±15		V
		TO-220	ISOWATT220	
I_D	Drain current (cont.) at $T_c=25°C$	15	10	A
I_D	Drain current (cont.) at $T_c=100°C$	9.5	6.3	A
I_{DM}(•)	Drain current (pulsed)	40	40	A
P_{tot}	Total dissipation at $T_c<25°C$	75	30	W
	Derating factor	0.6	0.24	W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj - case}$	Thermal resistance junction-case	max	1.67	4.16	°C/W
T_l	Maximum lead temperature for soldering purpose	max	275		°C

ELECTRICAL CHARACTERISTICS ($T_{case} = 25°C$ unless otherwise specified)

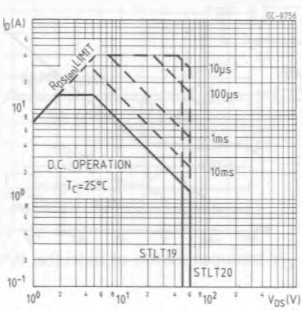
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu A$ $V_{GS} = 0$ for **STLT20/FI** for **STLT19/FI**	 60 50			 V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 $T_c = 125°C$			250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 15$ V			± 100	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu A$	1		2.5	V
$R_{DS\ (on)}$	Static drain-source on resistance	$V_{GS} = 5$ V $I_D = 7.5$ A			0.15	Ω
DYNAMIC						
g_{fs}	Forward transconductance	$V_{DS} = 15$ V $I_D = 7.5$ A	5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25$ V f = 1 MHz $V_{GS} = 0$		480 170 40		pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	$V_{DD} = 25$ V $I_D = 7.5$ A $V_i = 5$ V $R_i = 50\ \Omega$		10 70 35 40		ns ns ns ns
Q_g	Total Gate Charge	$V_{DD} = 48$ V $I_D = 15$ A $V_{GS} = 5$ V		8	13	nC

ELECTRICAL CHARACTERISTICS (Continued)

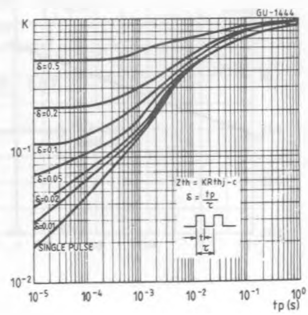
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}(•)	Source-drain current Source-drain current (pulsed)					15 60	A A
V_{SD}**	Forward on voltage	I_{SD} = 15 A	V_{GS} = 0			1.25	V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovered charge	I_{SD} = 15 A	di/dt = 100A/μs		80 0.15		ns μC

** Pulsed: Pulse duration ⩽ 300 μs, duty cycle ⩽ 2%
(•) Pulse width limited by safe operating area

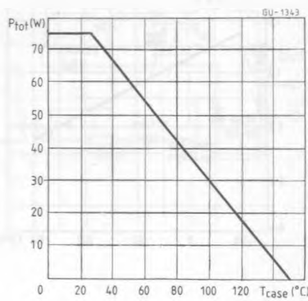
Safe operating areas (standard package)



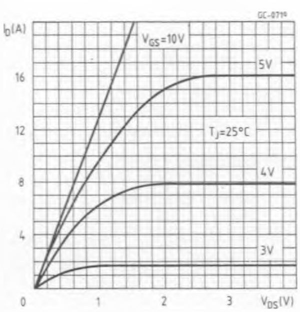
Thermal impedance (standard package)



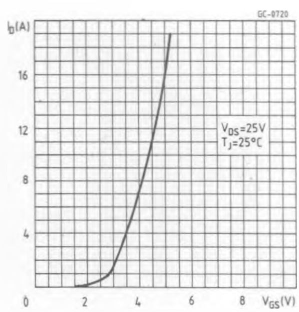
Derating curve (standard package)



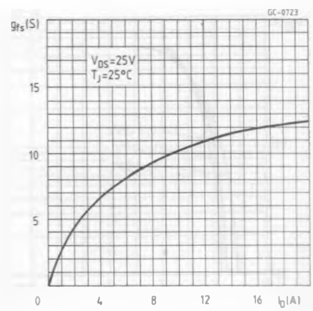
Output characteristics



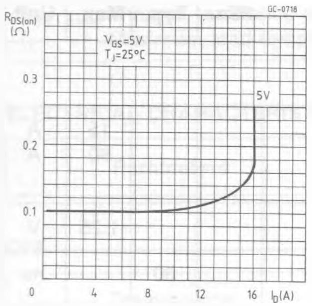
Transfer characteristics



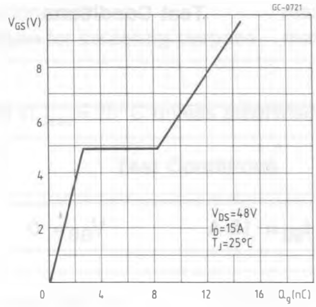
Transconductance



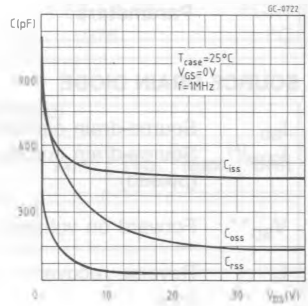
Static drain-source on resistance



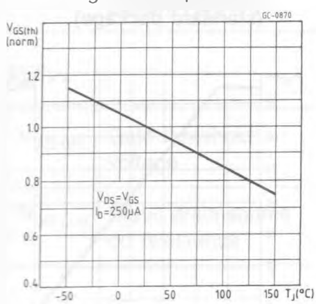
Gate charge vs gate-source voltage



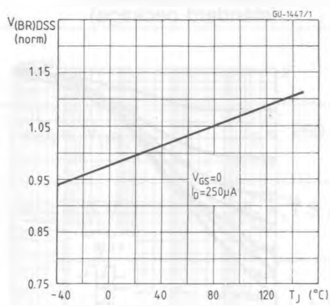
Capacitance variation



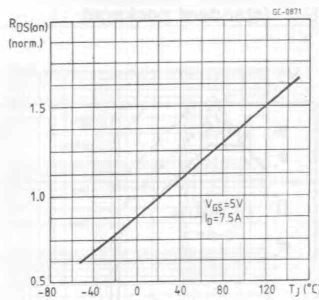
Normalized gate threshold voltage vs temperature



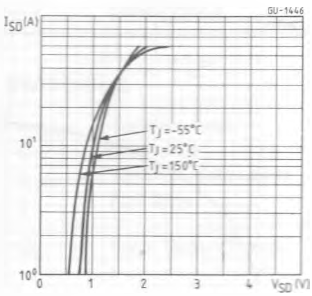
Normalized breakdown voltage vs temperature



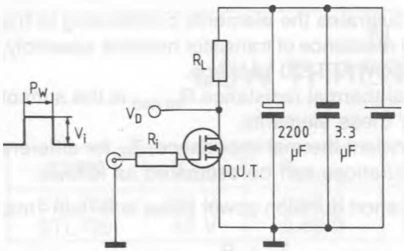
Normalized on resistance vs temperature



Source-drain diode forward characteristics

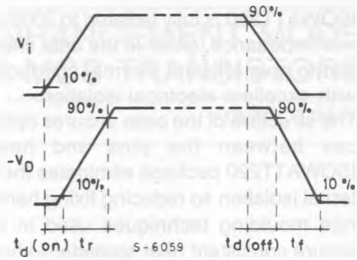


Switching times test circuit for resistive load

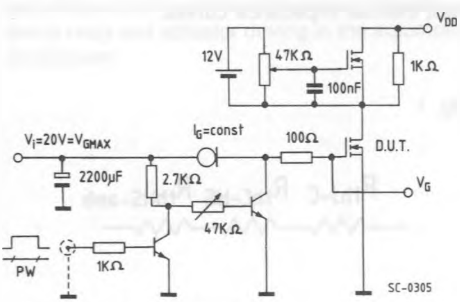


Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

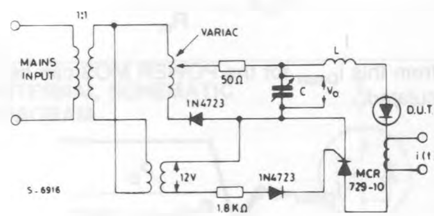


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)}\ (\text{at } 150°C)}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

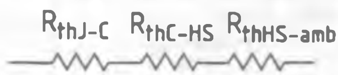
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

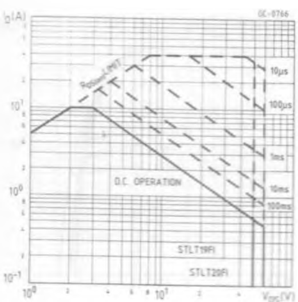
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

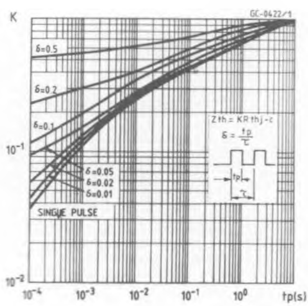


ISOWATT DATA

Safe operating areas



Thermal impedance



Derating curve