



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV _{DSS} /	R _{DS(ON)}	V _{GS(th)}	I _{D(ON)}	Order Number / F	Package
BV _{DGS}	(max)	(max)	(min)	TO-243AA*	Die [†]
100V	1.5Ω	2.0V	3.0A	TN2510N8	TN2510ND

^{*} Same as SOT-89. Product supplied on 2000 piece carrier tape reels.

Features

- □ Low threshold —2.0V max.
- ☐ High input impedance
- ☐ Low input capacitance 125pF max.
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Applications

- Logic level interfaces ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

^{*} Distance of 1.6 mm from case for 10 seconds.

Product marking for TO-243AA:

TN5A*

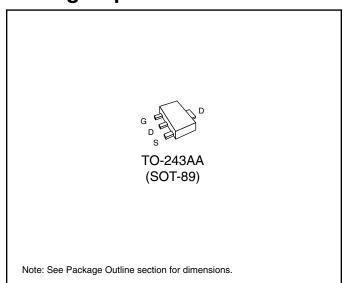
Where * = 2-week alpha date code

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option



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[†]MIL visual screening available.

Thermal Characteristics

Package	I _D (continuous)*	I _D (pulsed)	Power Dissipation @ T _A = 25°C	$ heta_{ extsf{jc}}$ °C/W	θ _{ja} °C/W	I _{DR} *	I _{DRM}	
TO-243AA	0.73A	5.0A	1.6W [†]	15	78 [†]	0.73A	5.0A	

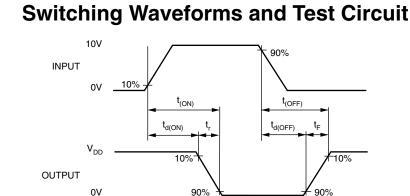
 $_{\perp}^{\star}$ I_D (continuous) is limited by max rated T_j.

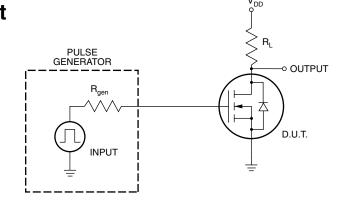
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Тур	Max	Unit	Conditions	
BV _{DSS}	Drain-to-Source Breakdown Voltage	100			V	$V_{GS} = 0V$, $I_D = 2mA$	
V _{GS(th)}	Gate Threshold Voltage	0.6		2.0	V	$V_{GS} = V_{DS}$, $I_D = 1mA$	
$\Delta V_{GS(th)}$	Change in V _{GS(th)} with Temperature			-4.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1.0 \text{mA}$	
I _{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
I _{DSS}	Zero Gate Voltage Drain Current			10	μΑ	$V_{GS} = 0V$, $V_{DS} = Max$ Rating	
				1.0	mA	$V_{GS} = 0V$, $V_{DS} = 0.8$ Max Rating $T_A = 125$ °C	
I _{D(ON)}	ON-State Drain Current	1.2	2.0		Α	$V_{GS} = 5.0V, V_{DS} = 25V$	
		3.0	6.0			$V_{GS} = 10V, V_{DS} = 25V$	
R _{DS(ON)}	Static Drain-to-Source			15		$V_{GS} = 3.0V, I_D = 250mA$	
	ON-State Resistance		1.5	2.0	Ω	V _{GS} = 4.5V, I _D = 750mA	
			1.0	1.5		$V_{GS} = 10V, I_D = 750mA$	
$\Delta R_{DS(ON)}$	Change in R _{DS(ON)} with Temperature			0.75	%/°C	$V_{GS} = 10V, I_D = 750mA$	
G _{FS}	Forward Transconductance	0.4	0.8		Ω	$V_{DS} = 25V, I_{D} = 1.0A$	
C _{ISS}	Input Capacitance		70	125		$V_{GS} = 0V$, $V_{DS} = 25V$ f = 1 MHz	
C _{OSS}	Common Source Output Capacitance		30	70	pF		
C _{RSS}	Reverse Transfer Capacitance		15	25			
t _{d(ON)}	Turn-ON Delay Time			10		V _{DD} = 25V,	
t _r	Rise Time			10	ns	$I_{D} = 1.5A,$	
t _{d(OFF)}	Turn-OFF Delay Time			20		$R_{GEN} = 25\Omega$	
t _f	Fall Time			10			
V _{SD}	Diode Forward Voltage Drop			1.8	V	$V_{GS} = 0V, I_{SD} = 1.5A$	
t _{rr}	Reverse Recovery Time		300		ns	V _{GS} = 0V, I _{SD} = 1.5A	

Notes:

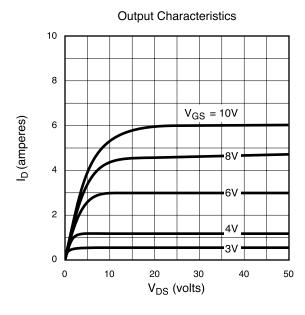
- 1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: $300\mu s$ pulse, 2% duty cycle.)
- 2. All A.C. parameters sample tested.

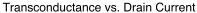


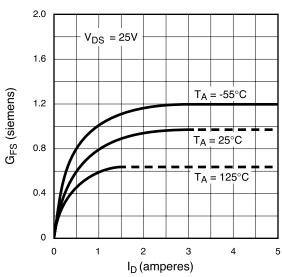


[†] Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_p increase possible on ceramic substrate.

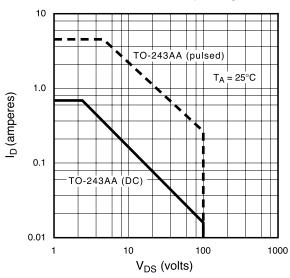
Typical Performance Curves



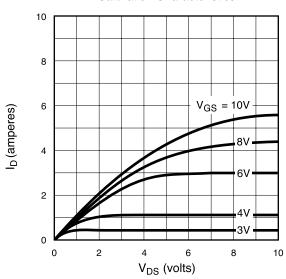




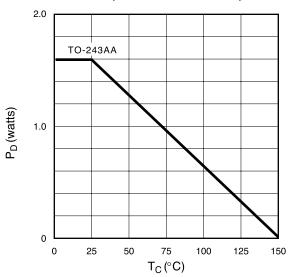
Maximum Rated Safe Operating Area



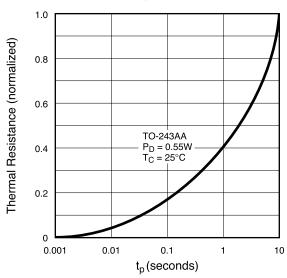
Saturation Characteristics



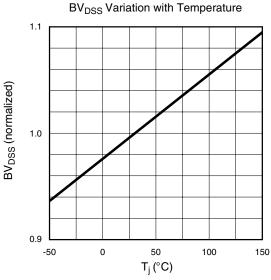
Power Dissipation vs. Ambient Temperature

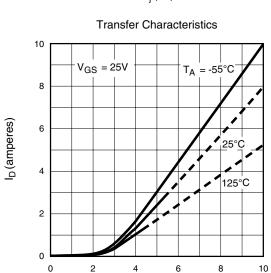


Thermal Response Characteristics

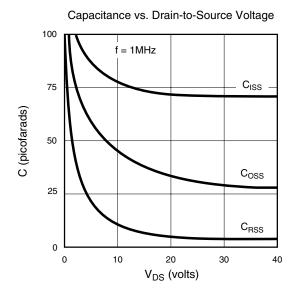


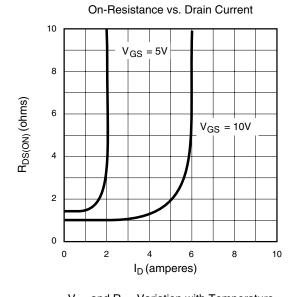
Typical Performance Curves

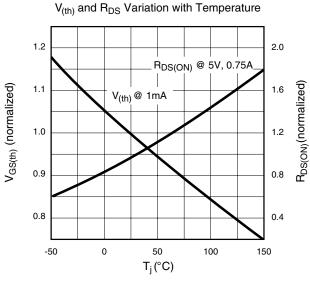


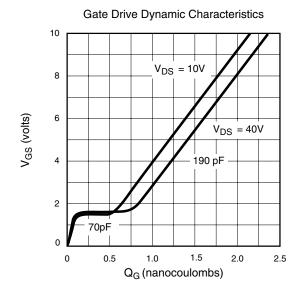


V_{GS} (volts)









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