TP2520
TP2522
Low Threshold

Supertex inc.

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-243AA*	Die†
-200V	12Ω	-2.4V	-0.75A	TP2520N8	—
-220V	12Ω	-2.4V	-0.75A	TP2522N8	TP2522ND

* Same as SOT-89. Product supplied on 2000 piece carrier tape reels.
† MIL visual screening available.

Product marking for TO-243AA

TP5C✻

Where ✻ = 2-week alpha date code

Features

- ❏ Low threshold — -2.4V max.
- ❏ High input impedance
- ❏ Low input capacitance — 125pF max.
- ❏ Fast switching speeds
- ❏ Low on resistance
- ❏ Free from secondary breakdown
- ❏ Low input and output leakage
- ❏ Complementary N- and P-channel devices

Applications

- ❏ Logic level interfaces – ideal for TTL and CMOS
- ❏ Solid state relays
- ❏ Battery operated systems
- ❏ Photo voltaic drives
- ❏ Analog switches
- ❏ General purpose line drivers
- ❏ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

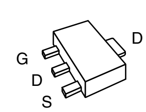
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option



TO-243AA
(SOT-89)

Note: See Package Outline section for dimensions.

11/12/01

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_A = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	-260mA	-2.0A	1.6W	15	78†	-260mA	-2.0A

* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

Electrical Characteristics (@ 25°C unless otherwise specified)

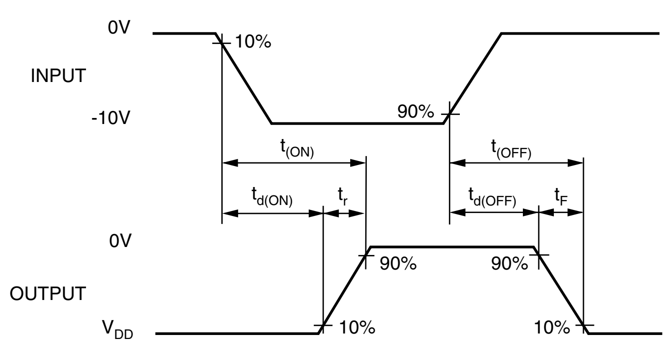
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage — TP2522	-220			V	$V_{GS} = 0V$, $I_D = -2mA$
	TP2520	-200				
$V_{GS(th)}$	Gate Threshold Voltage	-1.0		-2.4	V	$V_{GS} = V_{DS}$, $I_D = -1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			4.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1mA$
I_{GSS}	Gate Body Leakage			-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			-10	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
				-1.0	mA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	-0.25	-0.7		A	$V_{GS} = -4.5V$, $V_{DS} = -25V$
		-0.75	-2.1			$V_{GS} = -10V$, $V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		10	15	Ω	$V_{GS} = -4.5V$, $I_D = -100mA$
			8.0	12		$V_{GS} = -10V$, $I_D = -200mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.7	%/°C	$V_{GS} = -10V$, $I_D = -200mA$
G_{FS}	Forward Transconductance	100	250		m℧	$V_{DS} = -25V$, $I_D = -200mA$
C_{ISS}	Input Capacitance		75	125	pF	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance		20	85		
C_{RSS}	Reverse Transfer Capacitance		10	35		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = -25V$, $I_D = -0.75A$, $R_{GEN} = 25Ω$
t_r	Rise Time			15		
$t_{d(OFF)}$	Turn-OFF Delay Time			20		
t_f	Fall Time			15		
V_{SD}	Diode Forward Voltage Drop			-1.8	V	$V_{GS} = 0V$, $I_{SD} = -0.5A$
t_{rr}	Reverse Recovery Time		300		ns	$V_{GS} = 0V$, $I_{SD} = -0.5A$

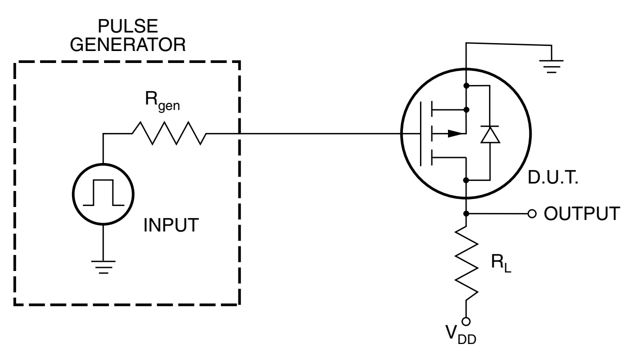
Notes:

1.All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

2.All A.C. parameters sample tested.

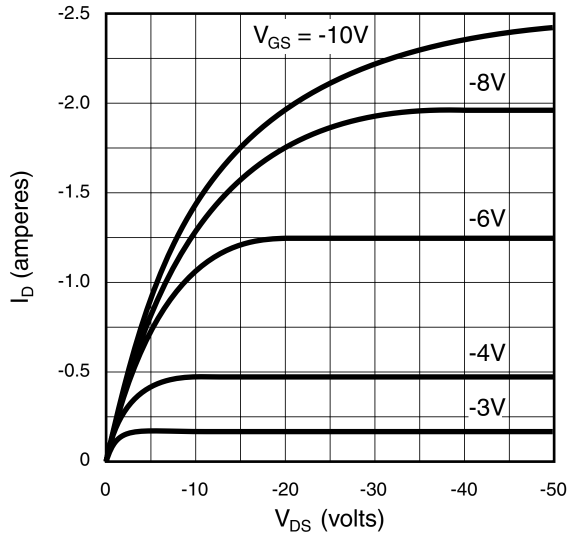
Switching Waveforms and Test Circuit



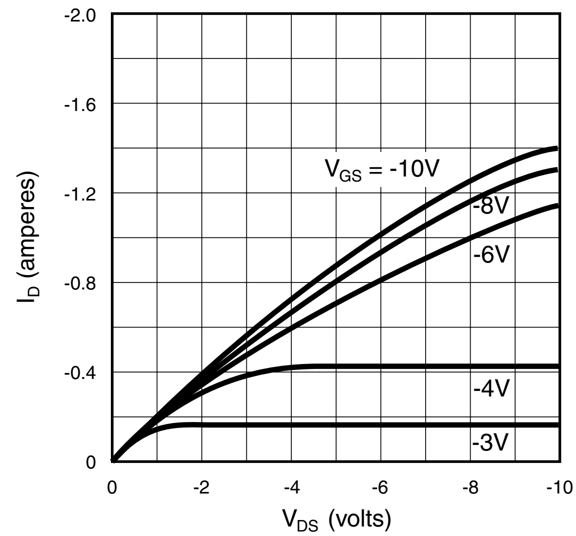


Typical Performance Curves

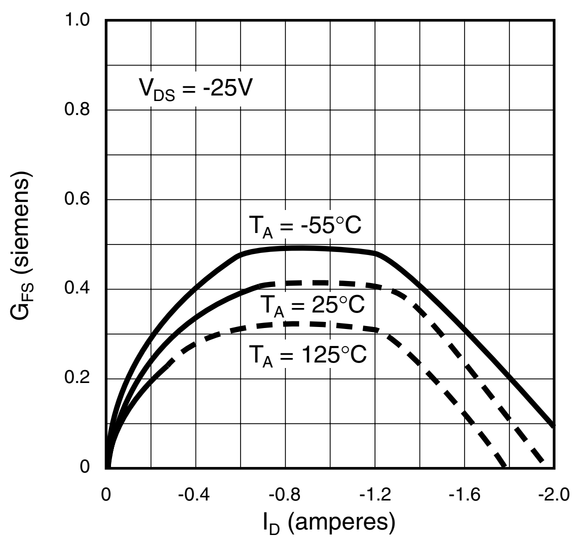
Output Characteristics



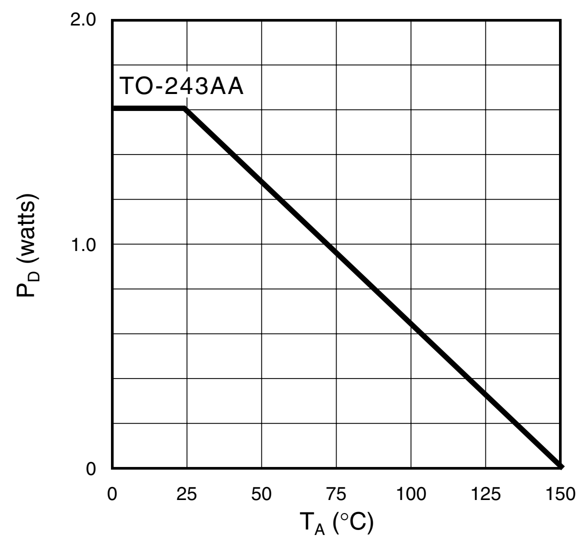
Saturation Characteristics



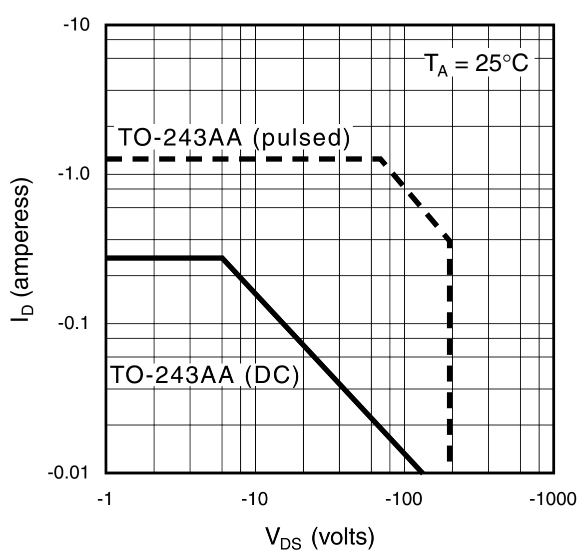
Transconductance vs. Drain Current



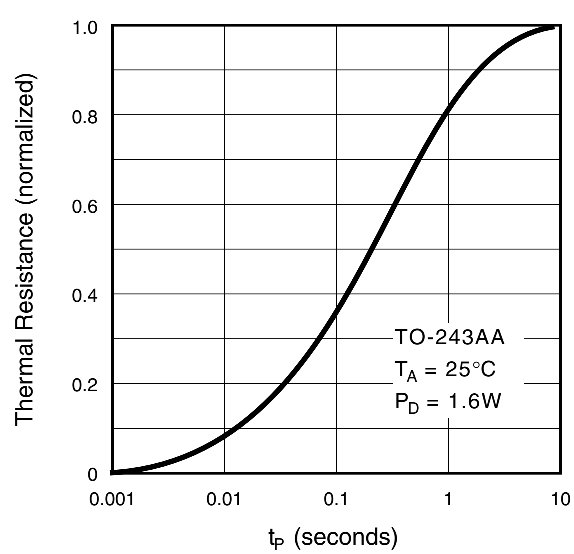
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area

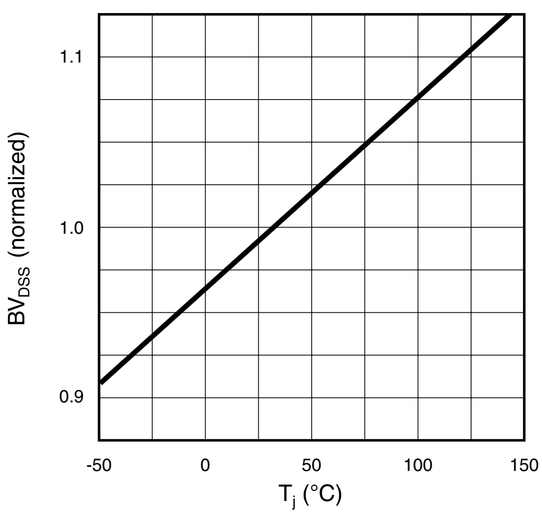


Thermal Response Characteristics

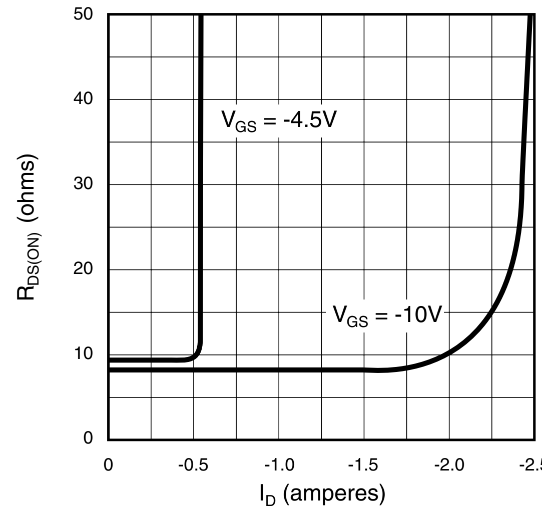


Typical Performance Curves

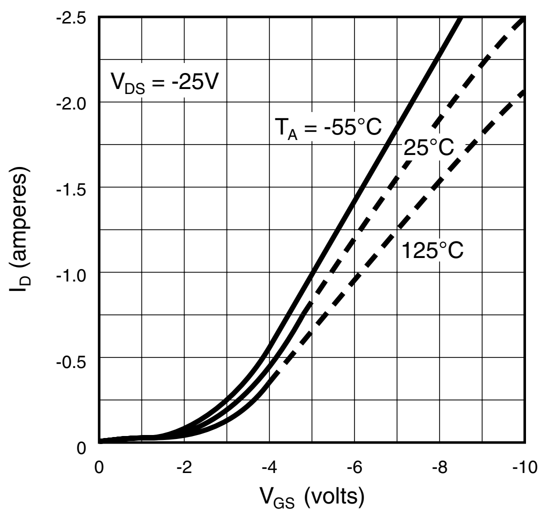
BV_{DSS} Variation with Temperature



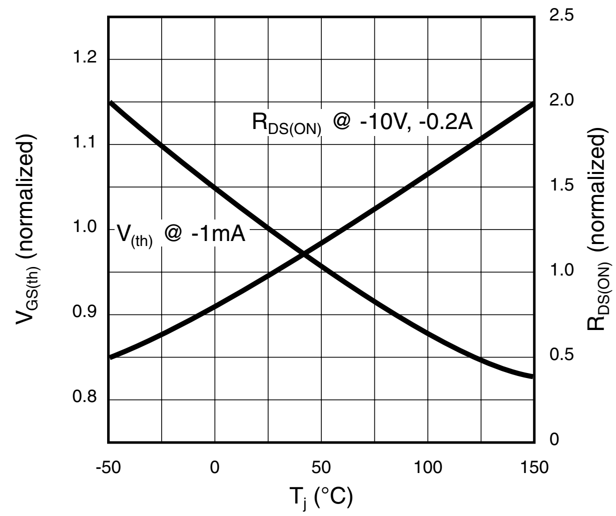
On-Resistance vs. Drain Current



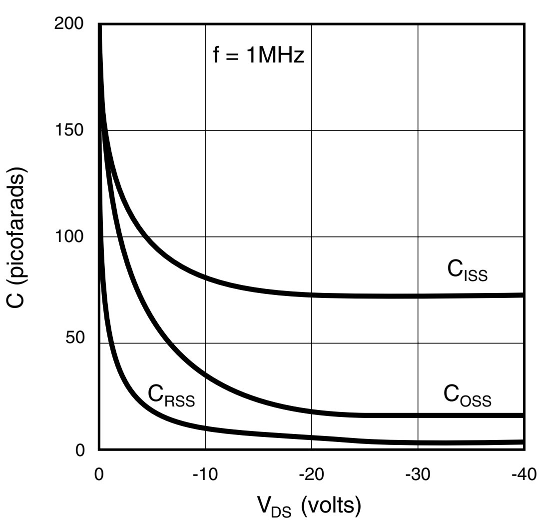
Transfer Characteristics



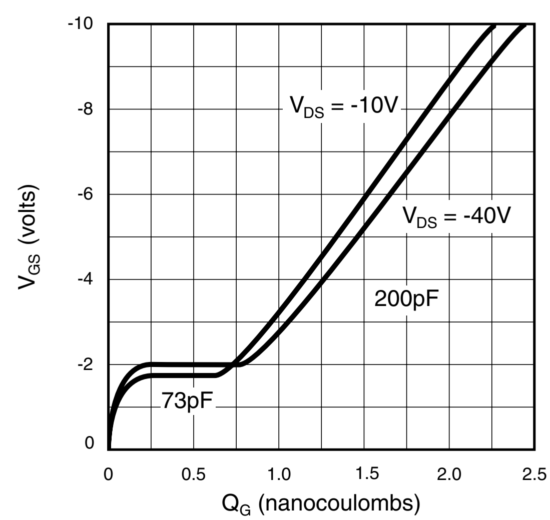
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



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