TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π-MOSV)

TPCS8004

High Speed Switching Applications
Switching Regulator Applications
DC-DC Converters

- Small footprint due to small and thin package
- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 0.56 Ω (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 1.8 S (typ.)
- Low leakage current: I_{DSS} = 100 μA (max) (V_{DS} = 200 V)
- Enhancement-model: V_{th} = 1.5~3.5 V (V_{DS} = 10 V, I_D = 1 mA)

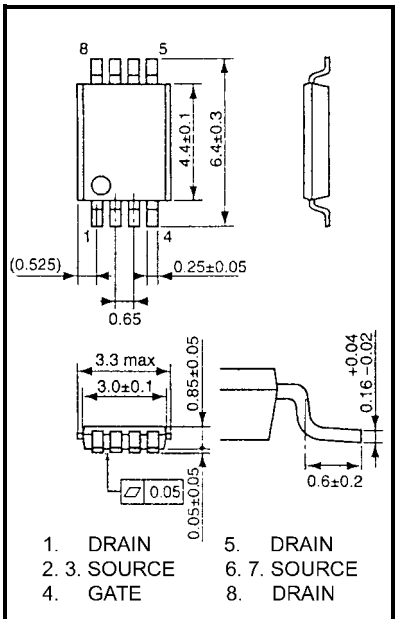
Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	200	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	200	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	1.3	A
	Pulse (Note 1)	I_{DP}	5.2	
Drain power dissipation (t = 10 s) (Note 2a)		P_D	1.5	W
Drain power dissipation (t = 10 s) (Note 2b)		P_D	0.6	
Single pulse avalanche energy(Note3)		E_{AS}	1.05	mJ
Avalanche current		I_{AR}	1.3	A
Repetitive avalanche energy (Note2a, Note 4)		E_{AR}	0.15	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note: For (Note 1), (Note 2), (Note 3) and (Note 4), please refer to the next page.

This transistor is an electrostatic sensitive device. Please handle with caution.

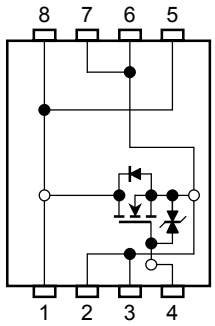
Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-3R1B

Weight: 0.035 g (typ.)

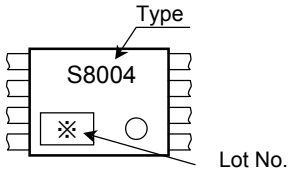
Circuit Configuration



Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	$R_{th\ (ch\text{-}a)}$	83.3	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	$R_{th\ (ch\text{-}a)}$	208	°C/W

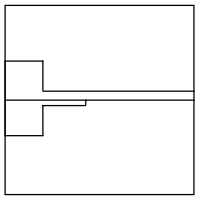
Marking (Note 5)



Note 1: Please use devices on condition that the channel temperature is below 150°C.

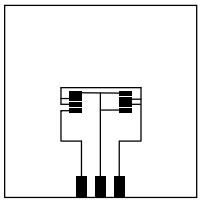
Note 2:

a) Device mounted on a glass-epoxy board (a)



FR-4
25.4 × 25.4 × 0.8
(unit: mm)

b) Device mounted on a glass-epoxy board (b)



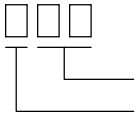
FR-4
25.4 × 25.4 × 0.8
(unit: mm)

Note 3: V_{DD} = 50 V, T_{ch} = 25°C (initial), L = 1.0 mH, R_G = 25 Ω, I_{AR} = 1.3 A

Note 4: Repetitive rating: pulse width limited by maximum channel temperature

Note 5: ○ on lower right of the marking indicates Pin 1.

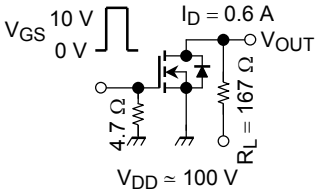
※ Weekly code: (Three digits)



Week of manufacture
(01 for first week of year, continues up to 52 or 53)

Year of manufacture
(One low-order digits of calendar year)

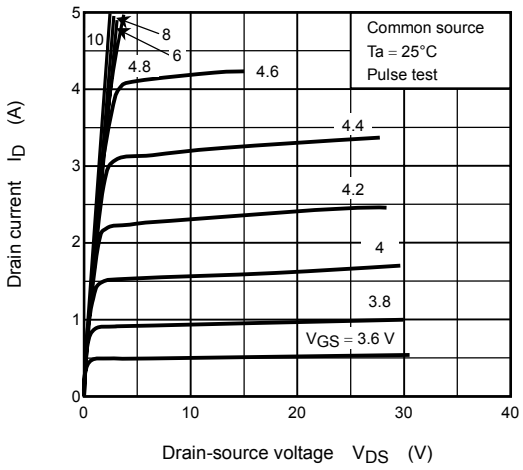
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-OFF current		I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	200	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	1.5	—	3.5	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 0.6 A	—	0.56	0.8	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 0.6 A	0.9	1.8	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	380	—	pF
Reverse transfer capacitance		C_{rss}		—	40	—	pF
Output capacitance		C_{oss}		—	140	—	pF
Switching time	Rise time	t_r		—	4.5	—	ns
	Turn-ON time	t_{on}		—	12	—	
	Fall time	t_f		—	23	—	
	Turn-OFF time	t_{off}	Duty ≦ 1%, t_w = 10 μs	—	54	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ 160 V, V_{GS} = 10 V, I_D = 1.3 A	—	12	—	nC
Gate-source charge		Q_{gs}		—	8	—	nC
Gate-drain (“miller”) charge		Q_{gd}		—	4	—	nC

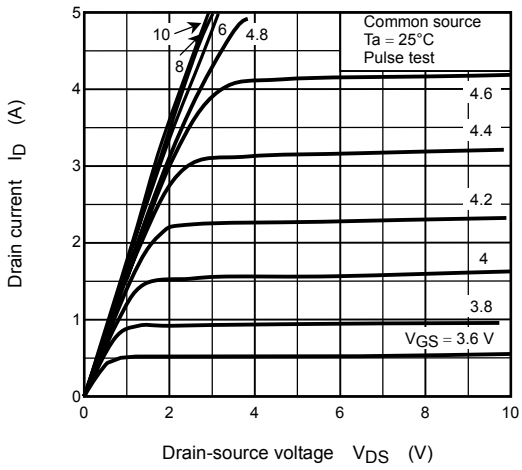
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current (pulse)	(Note 1)	I_{DRP}	—	—	—	5.2	A
Forward voltage (diode)		V_{DSF}	I_{DR} = 1.3 A, V_{GS} = 0 V	—	—	−2.0	V
Reverse recovery time		t_{rr}	I_{DR} = 1.3 A, V_{GS} = 0 V, dI_{DR}/dt = 100 A/μs	—	89	—	ns
Reverse recovery charge		Q_{rr}		—	230	—	nC

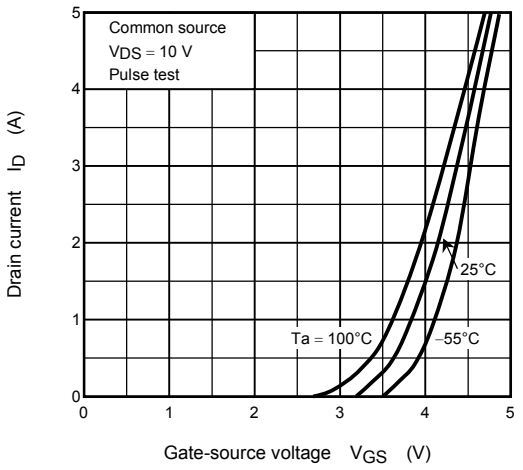
$I_D - V_{DS}$



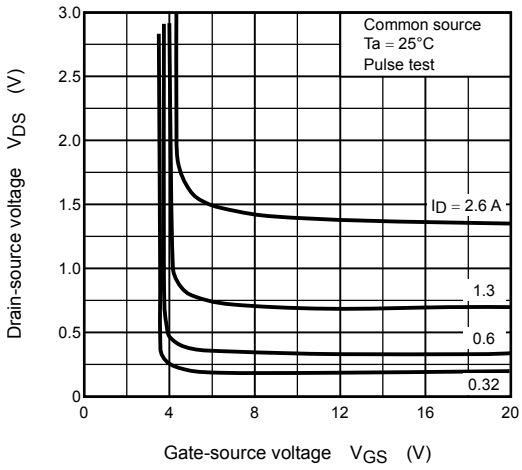
$I_D - V_{DS}$



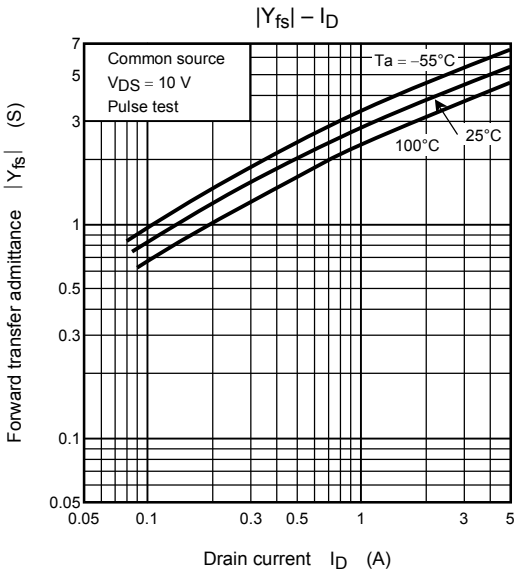
$I_D - V_{GS}$



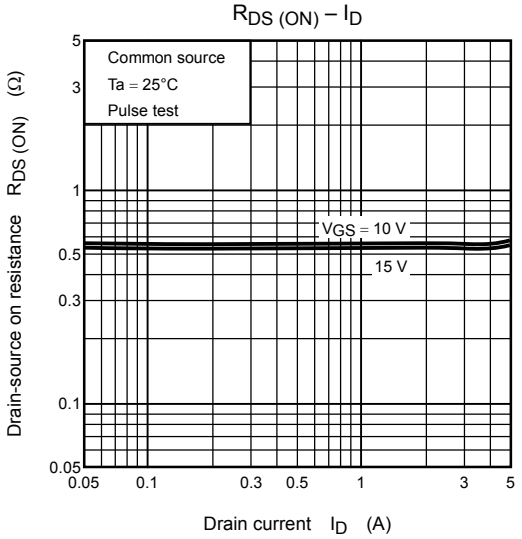
$V_{DS} - V_{GS}$



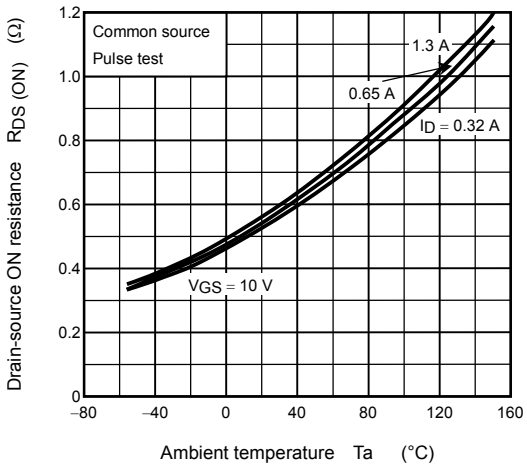
$|Y_{fs}| - I_D$



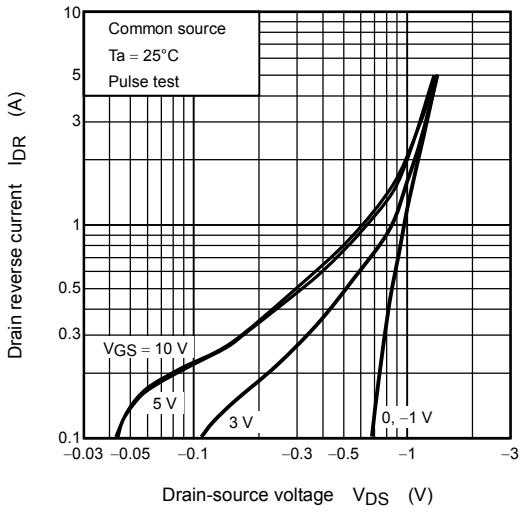
$R_{DS\ (ON)} - I_D$



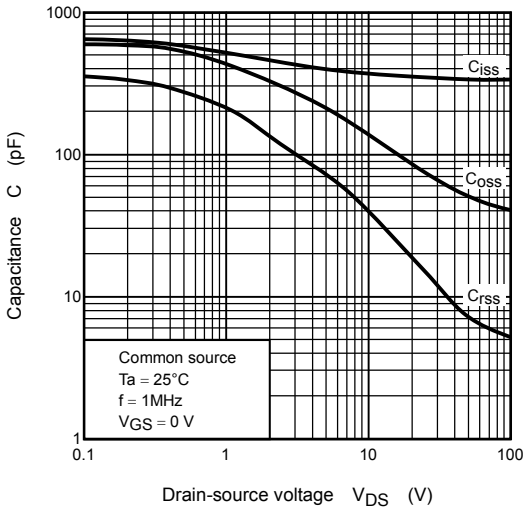
$R_{DS\ (ON)}$ – Ta



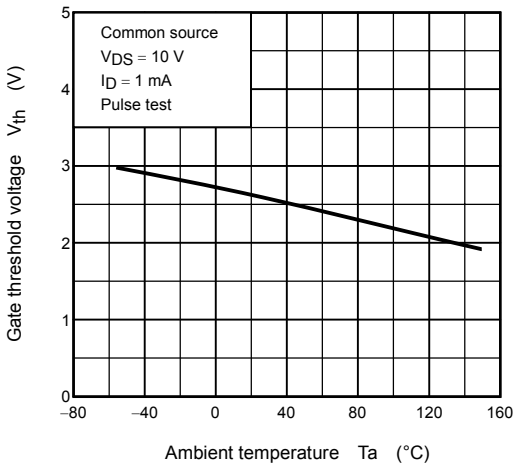
I_{DR} – V_{DS}



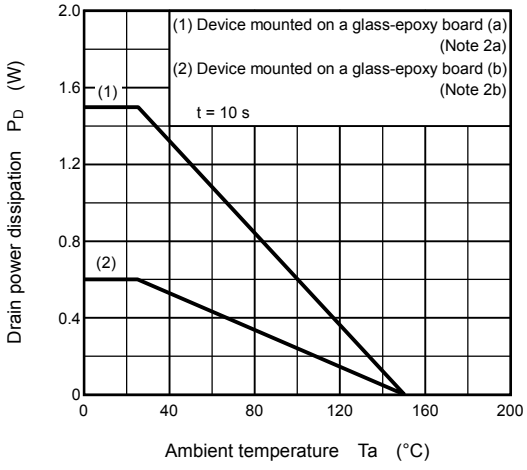
Capacitance – V_{DS}



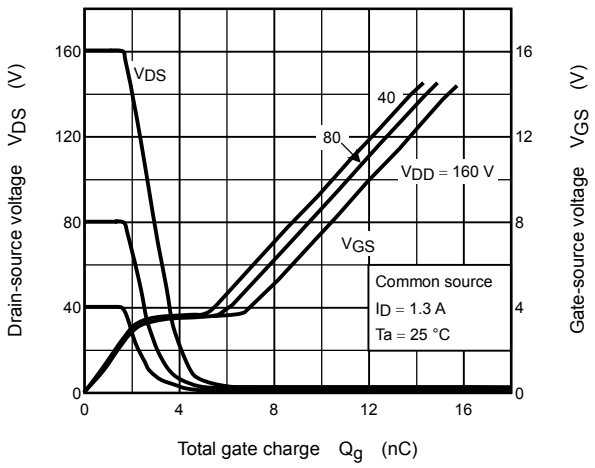
V_{th} – Ta



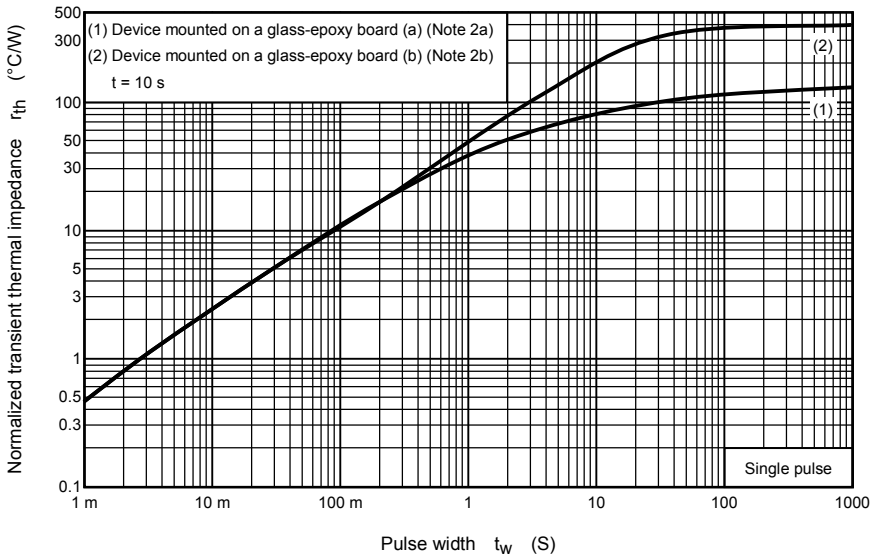
P_D – Ta



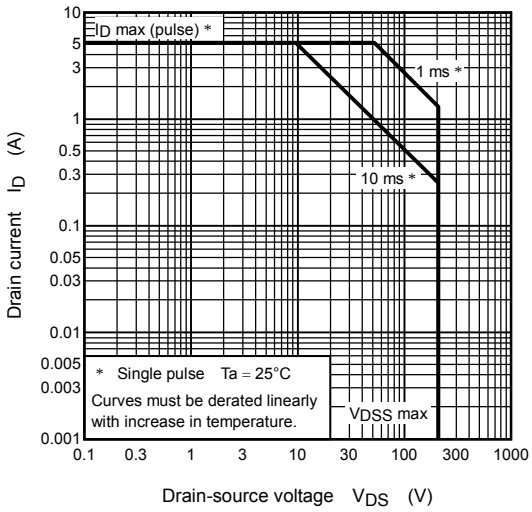
Dynamic input/output characteristics



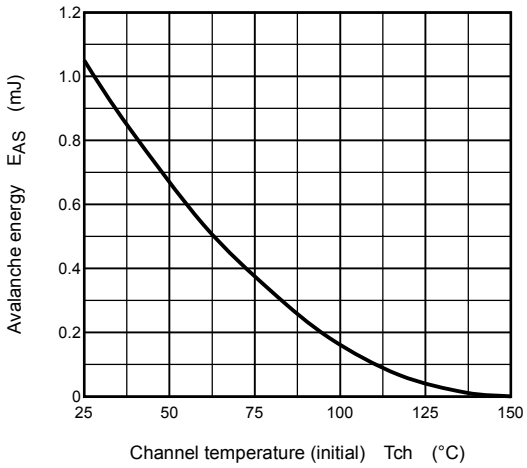
$r_{th} - t_w$

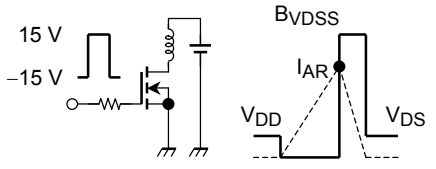


Safe operating area



$E_{AS} - T_{ch}$





Test circuit Wave form

T_{ch} = 25°C (Initial)
Peak I_{AR} = 1.3 A, R_G = 25 Ω
V_{DD} = 50 V, L = 1 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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