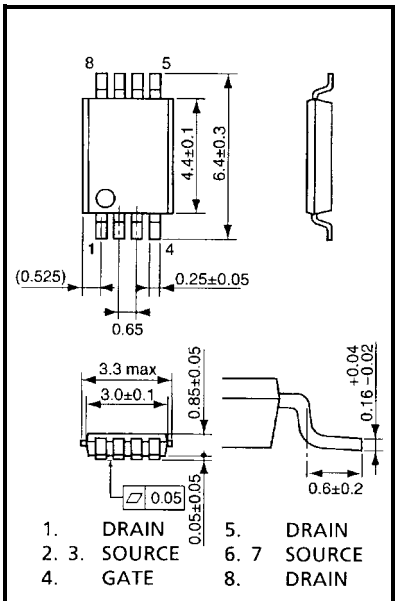
TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOS II)

TPCS8102

Lithium Ion Battery Applications
Portable Equipment Applications
Notebook PCs

- Small footprint due to small and thin package
- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 16 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 17 S (typ.)
- Low leakage current: I_{DSS} = −10 μA (max) (V_{DS} = −20 V)
- Enhancement-mode: V_{th} = −0.5~−1.2 V (V_{DS} = −10 V, I_D = −200 μA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-3R1B

Weight: 0.035 g (typ.)

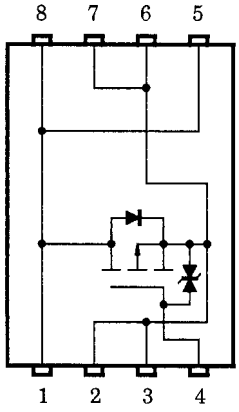
Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	−20	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	−20	V
Gate-source voltage		V_{GSS}	±12	V
Drain current	DC (Note 1)	I_D	−6	A
	Pulse (Note 1)	I_{DP}	−24	
Drain power dissipation (t = 10 s) (Note 2a)		P_D	1.5	W
Drain power dissipation (t = 10 s) (Note 2b)		P_D	0.6	W
Single pulse avalanche energy (Note 3)		E_{AS}	46.8	mJ
Avalanche current		I_{AR}	−6	A
Repetitive avalanche energy (Note 2a, Note 4)		E_{AR}	0.15	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: For (Note 1), (Note 2), (Note 3) and (Note 4), please refer to the next page.

This transistor is an electrostatic sensitive device. Please handle with caution.

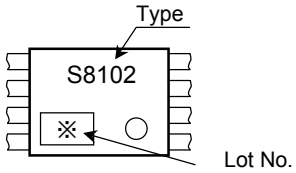
Circuit Configuration



Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	$R_{th\ (ch\text{-}a)}$	83.3	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	$R_{th\ (ch\text{-}a)}$	208	°C/W

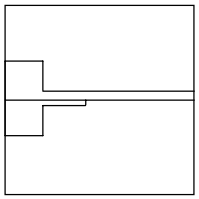
Marking (Note 5)



Note 1: Please use devices on condition that the channel temperature is below 150°C.

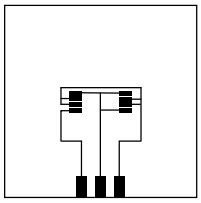
Note 2:

a) Device mounted on a glass-epoxy board (a)



FR-4
25.4 × 25.4 × 0.8
(unit: mm)

b) Device mounted on a glass-epoxy board (b)



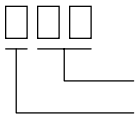
FR-4
25.4 × 25.4 × 0.8
(unit: mm)

Note 3: V_{DD} = −16 V, T_{ch} = 25°C (initial), L = 1.0 mH, R_G = 25 Ω, I_{AR} = −6.0 A

Note 4: Repetitive rating: pulse width limited by maximum channel temperature

Note 5: ○ on lower right of the marking indicates Pin 1.

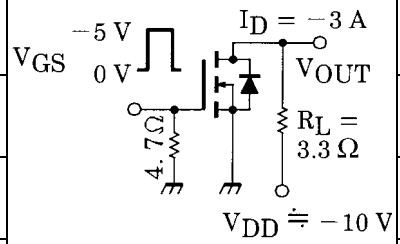
※ Weekly code: (Three digits)



Week of manufacture
(01 for first week of year, continues up to 52 or 53)

Year of manufacture
(One low-order digits of calendar year)

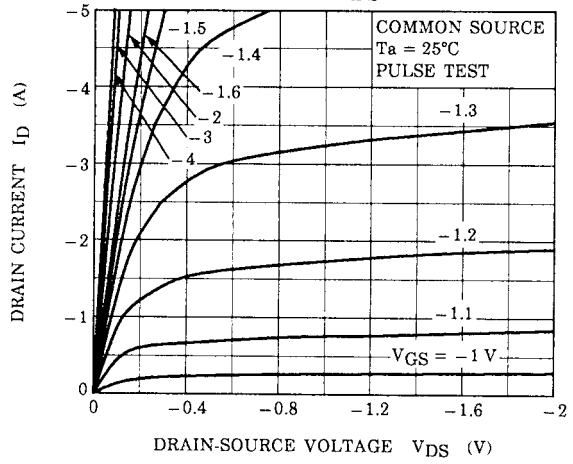
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-OFF current		I_{DSS}	V_{DS} = −20 V, V_{GS} = 0 V	—	—	−10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−20	—	—	V
		$V_{(BR)\ DSX}$	I_D = −10 mA, V_{GS} = 12 V	−8	—	—	
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −200 μA	−0.5	—	−1.2	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = −2.0 V, I_D = −3 A	—	30	60	mΩ
		$R_{DS\ (ON)}$	V_{GS} = −2.5 V, I_D = −3 A	—	23	38	
		$R_{DS\ (ON)}$	V_{GS} = −4 V, I_D = −3 A	—	16	20	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D = −3 A	8.5	17	—	S
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	2740	—	pF
Reverse transfer capacitance		C_{rss}		—	780	—	pF
Output capacitance		C_{oss}		—	1030	—	pF
Switching time	Rise time	t_r		—	7.6	—	ns
	Turn-ON time	t_{on}		—	16	—	
	Fall time	t_f		—	110	—	
	Turn-OFF time	t_{off}		—	230	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ −16 V, V_{GS} = −5 V, I_D = −6 A	—	37	—	nC
Gate-source charge		Q_{gs}		—	27	—	nC
Gate-drain (“miller”) charge		Q_{gd}		—	10	—	nC

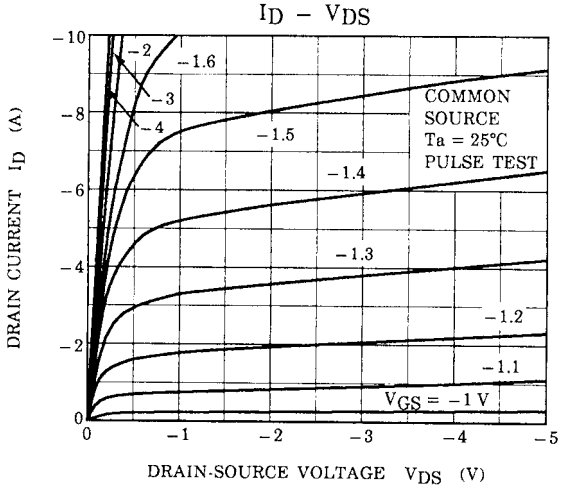
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	−24	A
Forward voltage (diode)		V_{DSF}	I_{DR} = −6 A, V_{GS} = 0 V	—	—	1.2	V

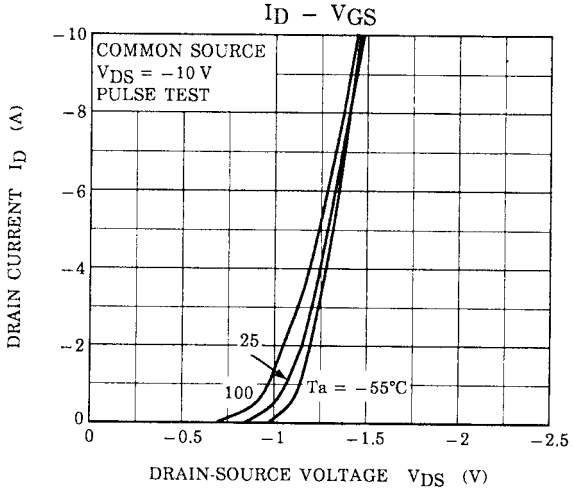
$I_D - V_{DS}$



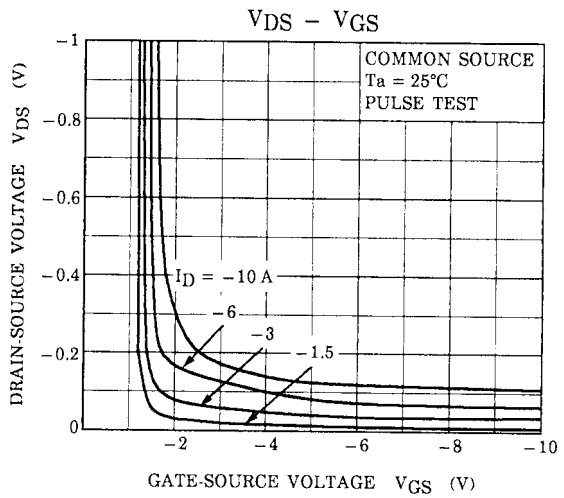
$I_D - V_{DS}$



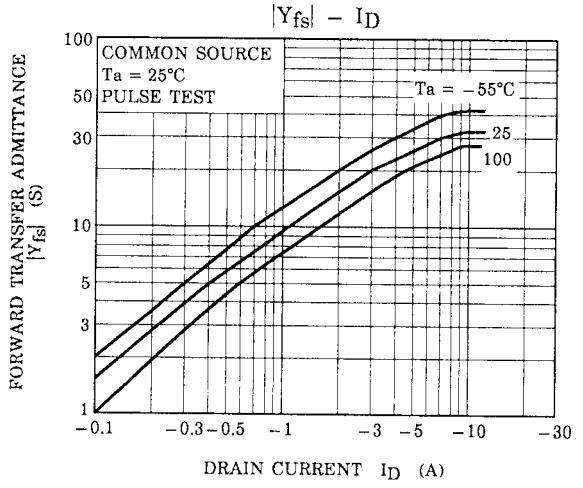
$I_D - V_{GS}$



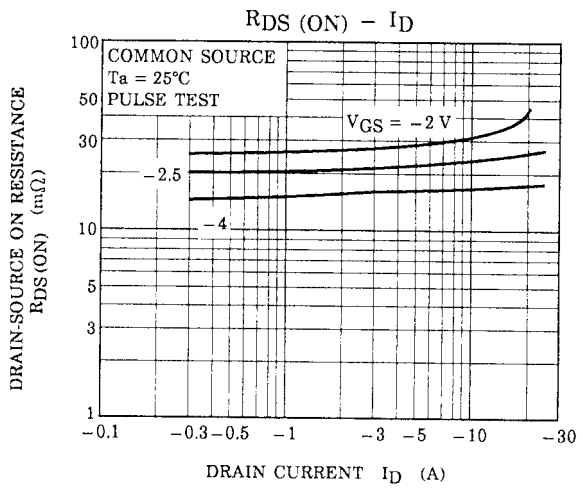
$V_{DS} - V_{GS}$



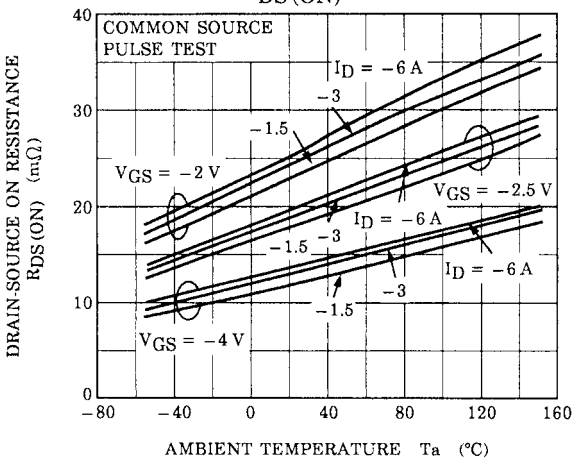
$|Y_{fs}| - I_D$



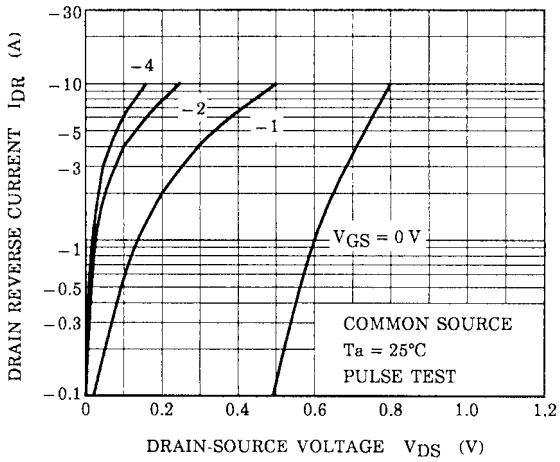
$R_{DS\ (ON)} - I_D$



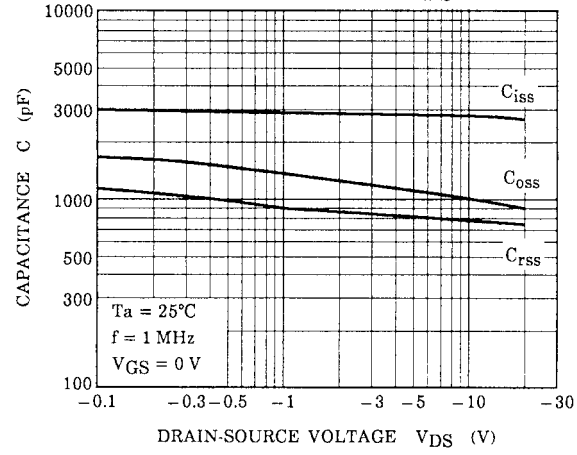
$R_{DS\,(ON)}$ – Ta



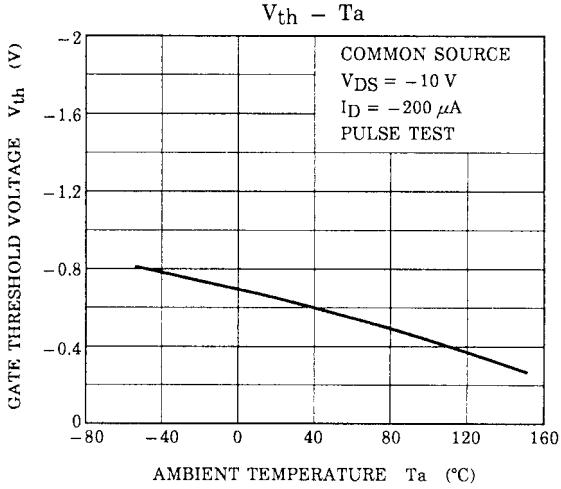
I_{DR} – V_{DS}



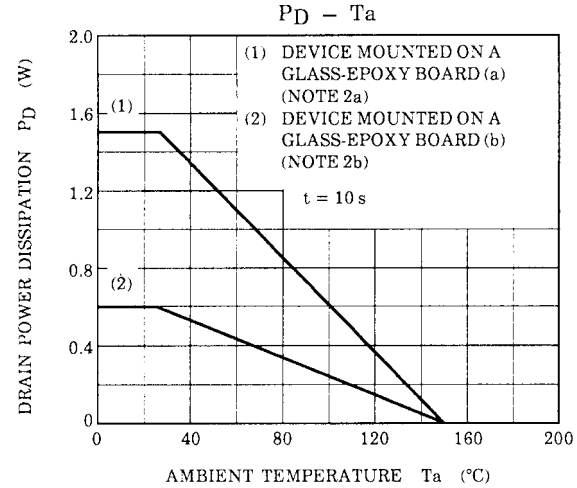
CAPACITANCE – V_{DS}



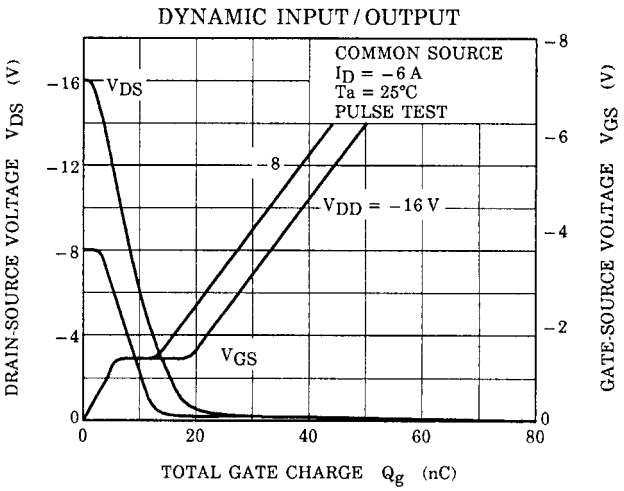
V_{th} – Ta



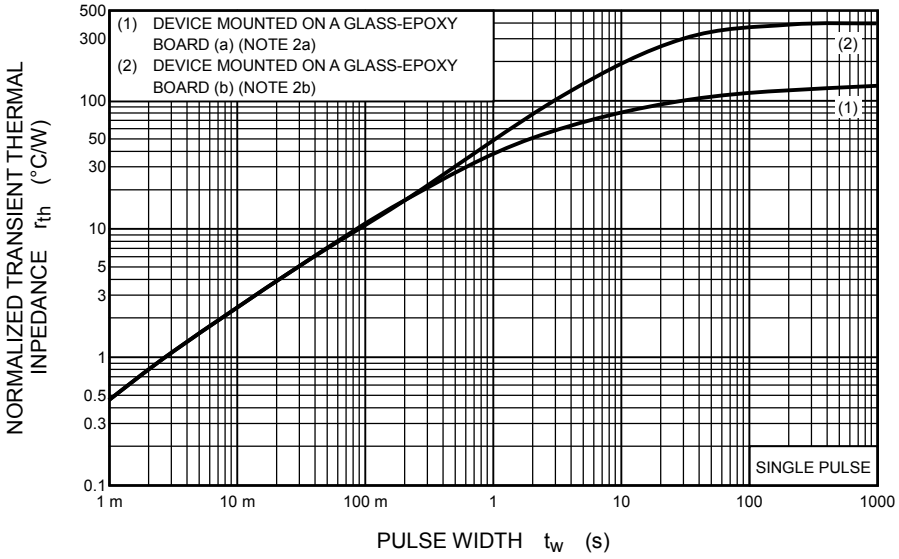
P_D – Ta



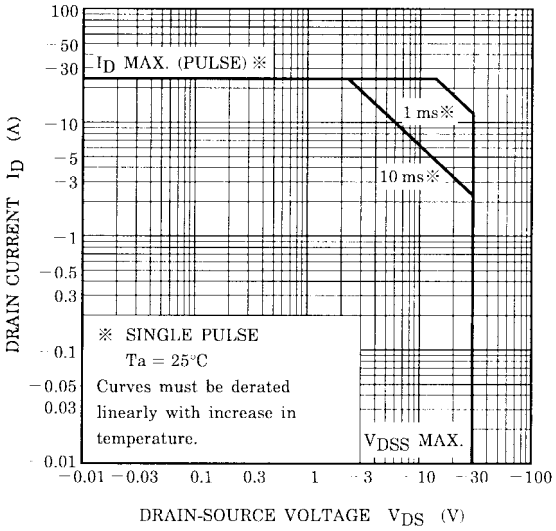
DYNAMIC INPUT / OUTPUT



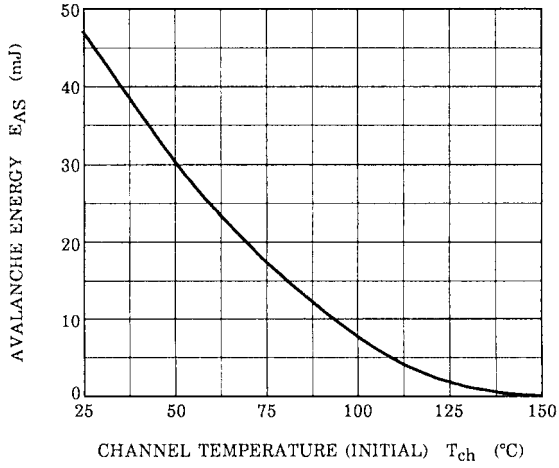
$r_{th} - t_w$

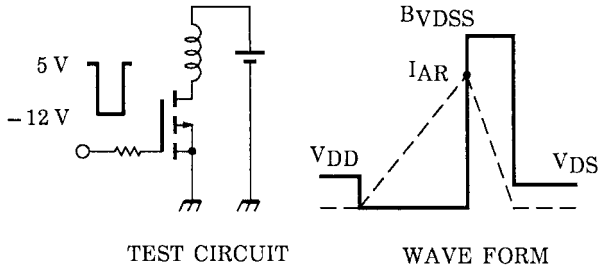


SAFE OPERATING AREA



$E_{AS} - T_{ch}$





TEST CIRCUIT WAVE FORM

T_{ch} = 25°C (Initial)
Peak I_{AR} = −6 A, R_G = 25 Ω $E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}}\right)$
V_{DD} = −16 V, L = 1.0 mH

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