



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	Order Number / Package	
			TO-39	TO-92
100V	0.35Ω	8A	VN2210N2	VN2210N3

† MIL visual screening available

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

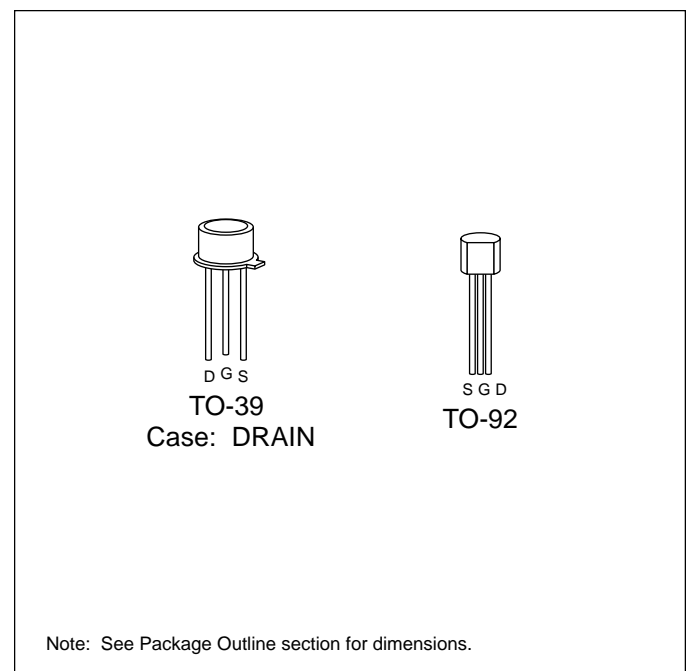
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{jc} $^\circ\text{C/W}$	θ_{ja} $^\circ\text{C/W}$	I_{DR}^*	I_{DRM}
TO-92	1.2A	8.0A	1.0W	125	170	1.2A	8.0A
TO-39	1.7A	10.0A	6.0W	21	125	1.7A	10.0A

* I_D (continuous) is limited by max rated T_j .

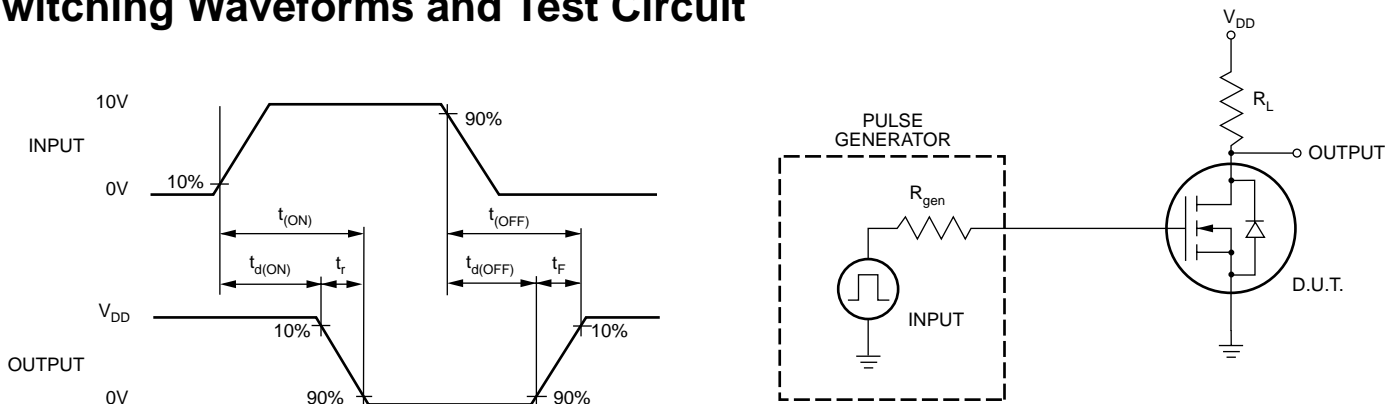
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100			V	$V_{GS} = 0V, I_D = 10mA$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.4	V	$V_{GS} = V_{DS}, I_D = 10mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-4.3	-5.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 10mA$
I_{GSS}	Gate Body Leakage		1	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			50	μA	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
				10	mA	$V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	3	4.5		A	$V_{GS} = 5V, V_{DS} = 25V$
		8	17			$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		0.4	0.5	Ω	$V_{GS} = 5V, I_D = 1A$
			0.27	0.35		$V_{GS} = 10V, I_D = 4A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.85	1.2	%/ $^\circ\text{C}$	$V_{GS} = 10V, I_D = 4A$
G_{FS}	Forward Transconductance	1.2			S	$V_{DS} = 25V, I_D = 2A$
C_{ISS}	Input Capacitance		300	500	pF	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance		125	200		
C_{RSS}	Reverse Transfer Capacitance		50	65		
$t_{d(ON)}$	Turn-ON Delay Time		10	15	ns	$V_{DD} = 25V$ $I_D = 2A$ $R_{GEN} = 10\Omega$
t_r	Rise Time		10	15		
$t_{d(OFF)}$	Turn-OFF Delay Time		50	65		
t_f	Fall Time		30	50		
V_{SD}	Diode Forward Voltage Drop		1.0	1.6	V	$V_{GS} = 0V, I_{SD} = 4A$
t_{rr}	Reverse Recovery Time		500		ns	$V_{GS} = 0V, I_{SD} = 1A$

Notes:

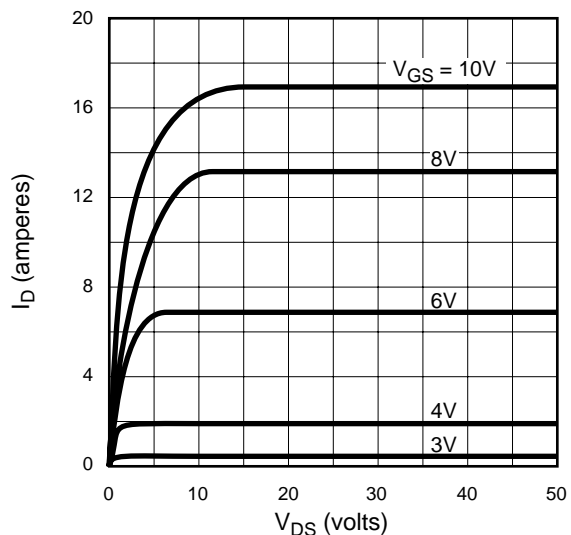
- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: $300\mu\text{s}$ pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

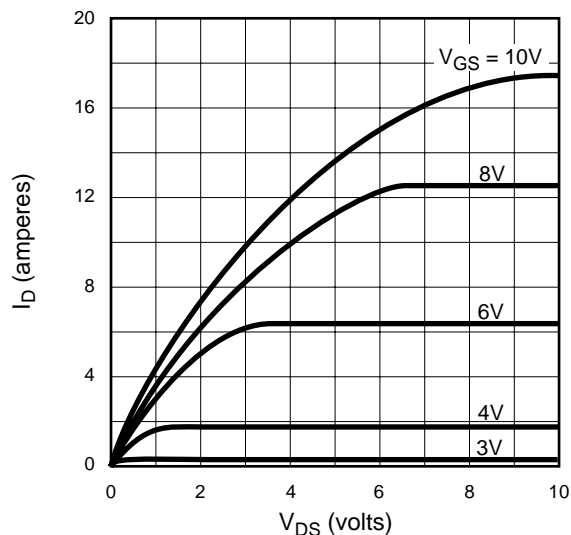


Typical Performance Curves

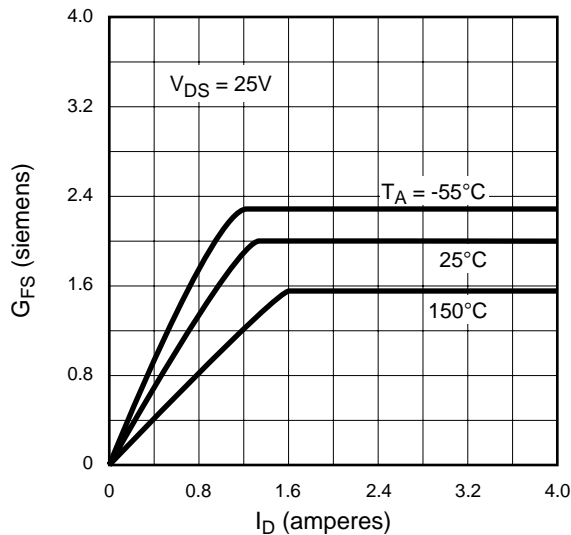
Output Characteristics



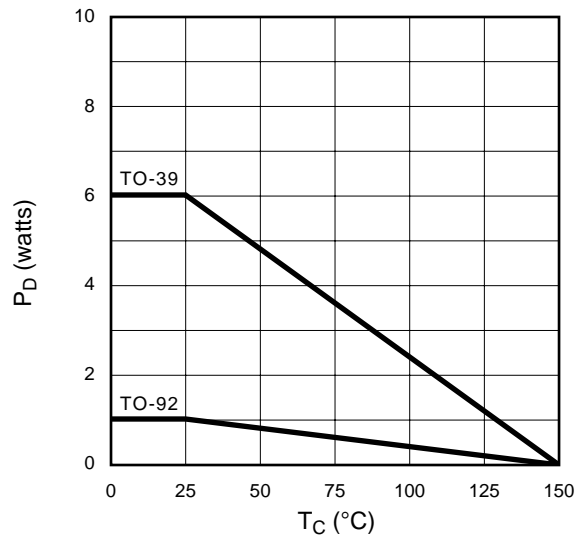
Saturation Characteristics



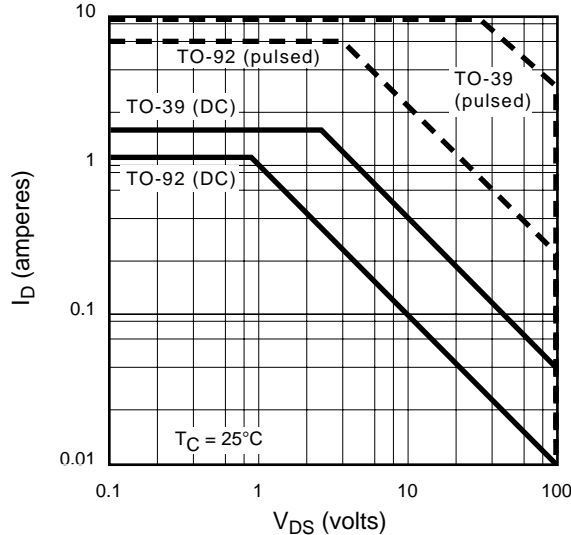
Transconductance vs. Drain Current



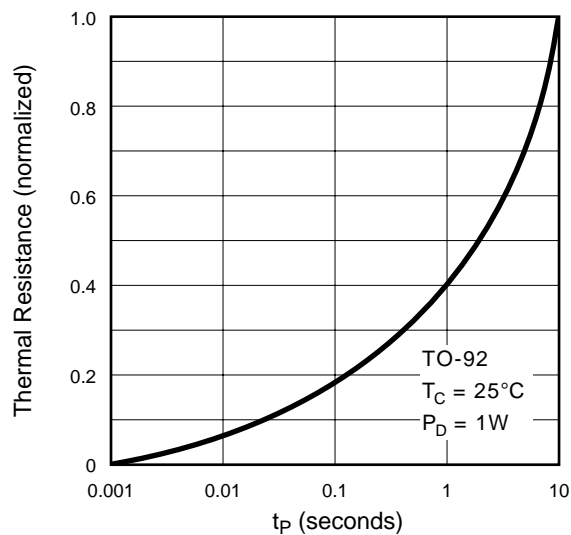
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



Typical Performance Curves

