

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV _{DSS} /	R _{DS(ON)}	I _{D(ON)}	Order Number / Package		
BV _{DGS}	(max)	(min)	TO-92		
-80V	5.0Ω	-1.1A	VP0808L		

Features

- ☐ Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{iss} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- ☐ High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

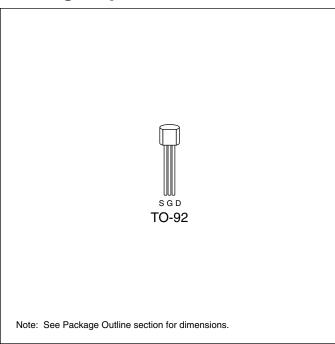
^{*} Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option



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Thermal Characteristics

Package	I _D (continuous)*	I _D (pulsed)	Power Dissipation	$^{ heta_{ extsf{jc}}}$ $^{\circ}$ C/W	$ heta_{ja}$ °C/W
TO-92	-0.28A	-3A	1W	125	170

 $^{^{\}star}$ $\rm I_{\rm D}$ (continuous) is limited by max rated $\rm T_{\rm j}.$

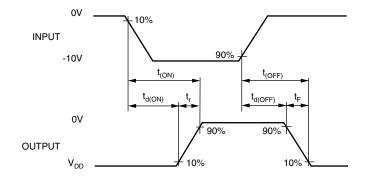
Electrical Characteristics (@ 25°C unless otherwise specified)

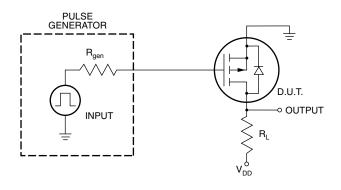
Symbol	Parameter	Min	Тур	Max	Unit	Conditions	
BV _{DSS}	Drain-to-Source Breakdown Voltage	-80			V	V_{GS} = 0V, I_D =-10 μ A	
V _{GS(th)}	Gate Threshold Voltage	-1.0		-4.5	V	$V_{GS} = V_{DS}$, $I_D = -1mA$	
I _{GSS}	Gate Body Leakage			-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
I _{DSS}	Zero Gate Voltage Drain Current			-10		$V_{GS} = 0V$, $V_{DS} = Max$ Rating	
				-500	μΑ	$V_{GS} = 0V$, $V_{DS} = Max$ Rating $T_A = 125$ °C	
I _{D(ON)}	ON-State Drain Current	-1.1			А	$V_{GS} = -10V, V_{DS} = -15V$	
R _{DS(ON)}	Static Drain-to-Source ON-State Resistance			5.0	Ω	$V_{GS} = -10V, I_D = -1A$	
G _{FS}	Forward Transconductance	200			m℧	$V_{DS} = -10V, I_{D} = -0.5A$	
C _{ISS}	Input Capacitance			150			
C _{OSS}	Common Source Output Capacitance			60	pF	$V_{GS} = 0V, V_{DS} = -25V$ f = 1MHz	
C _{RSS}	Reverse Transfer Capacitance			25		1 – 1141112	
t _{d(ON)}	Turn-ON Delay Time			15			
t _r	Rise Time			40		$V_{DD} = -25V$, $I_{D} = -0.5A$ $R_{GEN} = 25\Omega$	
t _{d(OFF)}	Turn-OFF Time			30	ns		
t _f	Fall Time			30			
V _{SD}	Diode Forward Voltage Drop		-1.2		V	$V_{GS} = 0V, I_{SD} = -0.9A$	

Notes:

- 1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: $300\mu s$ pulse, 2% duty cycle.)
- 2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





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