XN01872 (XN1872)

Silicon N-channel • Enhancement MOS FET

For switching

Features

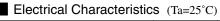
- Two elements incorporated into one package. (Source-coupled FETs)
- Reduction of the mounting area and assembly cost by one half.

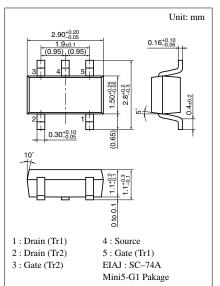
Basic Part Number of Element

• 2SK0621(2SK621) × 2 elements

Parameter		Symbol	Ratings	Unit		
Rating of element	Drain to source voltage	V _{DSS}	50	V		
	Gate to source voltage	V _{GSO}	8	V		
	Drain current	ID	100	mA		
		I_{DM}	200	mA		
Overall	Total power dissipation	P _T	300	mW		
	Channel temperature	T _{ch}	150	°C		
	Storage temperature	T _{stg}	-55 to +150	°C		

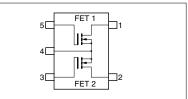
Absolute Maximum Ratings (Ta=25°C)





Marking Symbol: 5U

Internal Connection

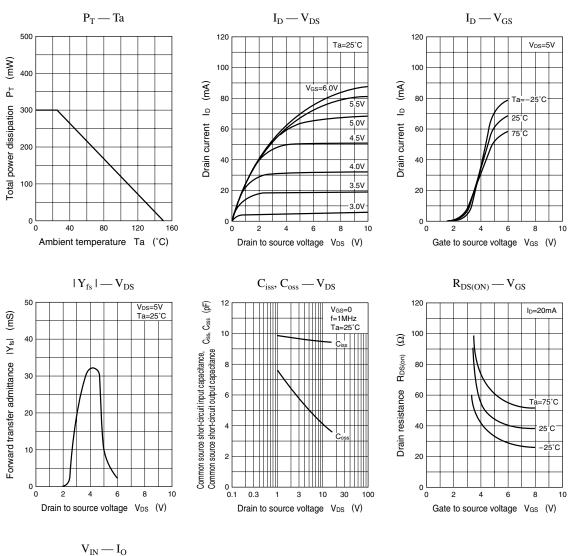


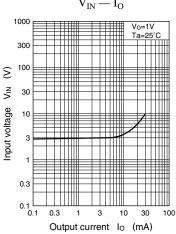
Parameter	Symbol	Conditions	min	typ	max	Unit
Drain to source voltage	V _{DSS}	$I_D = 100 \mu A, V_{GS} = 0$	50			V
Drain current	I _{DSS}	$V_{DS} = 10V, V_{GS} = 0$			10	μΑ
Gate cutoff current	I _{GSS}	$V_{GS} = 8V, V_{DS} = 0$	40		80	μΑ
Gate threshold voltage	V _{th}	$I_D = 100 \mu A, V_{DS} = V_{GS}$	1.5		3.5	V
Drain resistance	R _{DS(on)}	$I_D = 20 \text{mA}, V_{GS} = 5 \text{V}$			50	Ω
Forward transfer admittance	Y _{fs}	$I_D = 20 \text{mA}, V_{DS} = 5 \text{V}, f = 1 \text{kHz}$	20	30		mS
Output voltage high level	V _{OH}	$V_{DS} = 5V, V_{GS} = 1V, R_L = 200\Omega$	4.5			V
Output voltage low level	V _{OL}	$V_{DS} = 5V, V_{GS} = 5V, R_L = 200\Omega$			1.0	V
Input resistance	$R_1 + R_2^{*1}$		100		200	kΩ
Turn-on time	ton*2	V_{DD} = 5V, V_{GS} = 0 to 5V, R_L = 200 Ω			1.0	μs
Turn-off time	t _{off} *2	V_{DD} = 5V, V_{GS} = 5 to 0V, R_L = 200 Ω			1.0	μs
Common source short-circuit input capacitance	C _{iss}	$V_{DS} = 5V, V_{GS} = 0, f = 1MHz$		9	15	pF

*1 Pulse measurement

^{*2} Resistance ratio $R_1/R_2 = 1/50$

Note) The Part number in the Parenthesis shows conventional part number.





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