# XP05553

## Silicon NPN epitaxial planar transistor

#### For low-frequency amplification

#### ■ Features

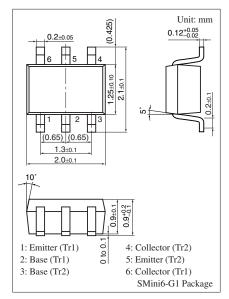
- Two elements incorporated into one package (Each transistor is separated)
- Reduction of the mounting area and assembly cost by one half
- $\bullet$  High forward current transfer ratio  $h_{\text{FE}}$

#### ■ Basic Part Number of Element

•  $2SD1149 \times 2$  elements

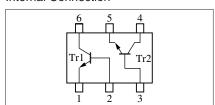
## $\blacksquare$ Absolute Maximum Ratings $T_a = 25^{\circ}C$

Parameter		Symbol	Rating	Unit	
Rating of	Collector-base voltage (Emitter open)	V <sub>CBO</sub>	100	V	
element	Collector-emitter voltage (Base open)	V <sub>CEO</sub>	100	V	
	Emitter-base voltage (Collector open)	V <sub>EBO</sub>	15	V	
	Collector current	$I_C$	20	mA	
Overall	Total power dissipation	$P_{T}$	150	mW	
	Junction temperature	$T_j$	150	°C	
	Storage temperature	T <sub>stg</sub>	-55 to +150	°C	



Marking Symbol: 4U

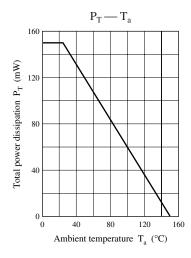
#### Internal Connection

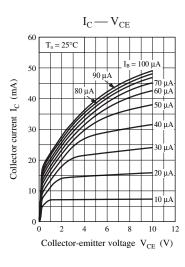


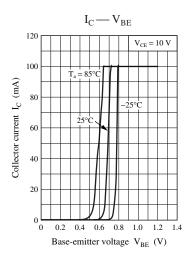
### ■ Electrical Characteristics $T_a = 25$ °C $\pm 3$ °C

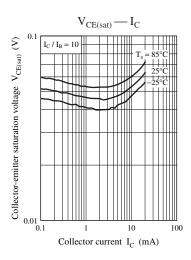
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Collector-base voltage (Emitter open)	V <sub>CBO</sub>	$I_C = 10 \ \mu A, I_E = 0$	100			V
Collector-emitter voltage (Base open)	V <sub>CEO</sub>	$I_C = 1 \text{ mA}, I_B = 0$	100			V
Emitter-base voltage (Collector open)	$V_{EBO}$	$I_E = 10 \ \mu A, I_C = 0$	15			V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = 60 \text{ V}, I_{E} = 0$			0.1	μΑ
Collector-emitter cutoff current (Base open)	$I_{CEO}$	$V_{CE} = 60 \text{ V}, I_{B} = 0$			1	μΑ
Forward current transfer ratio	$h_{FE}$	$V_{CE} = 10 \text{ V}, I_{C} = 2 \text{ mA}$	400		2000	_
Collector-emitter saturation voltage	V <sub>CE(sat)</sub>	$I_C = 10 \text{ mA}, I_B = 1 \text{ mA}$		0.05	0.20	V
Noise voltage	NV	$V_{CE} = 10 \text{ V}, I_{C} = 1 \text{ mA}, G_{V} = 80 \text{ dB}$		80		mV
		$R_g = 100 \text{ k}\Omega$ , Function = Flat				
Transition frequency	$f_T$	$V_{CB} = 10 \text{ V}, I_E = -2 \text{ mA}, f = 200 \text{ MHz}$		150		MHz

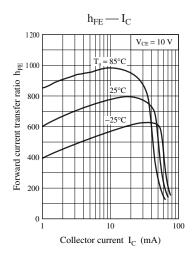
Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

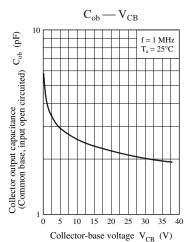












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