

### PACKAGE OUTLINE

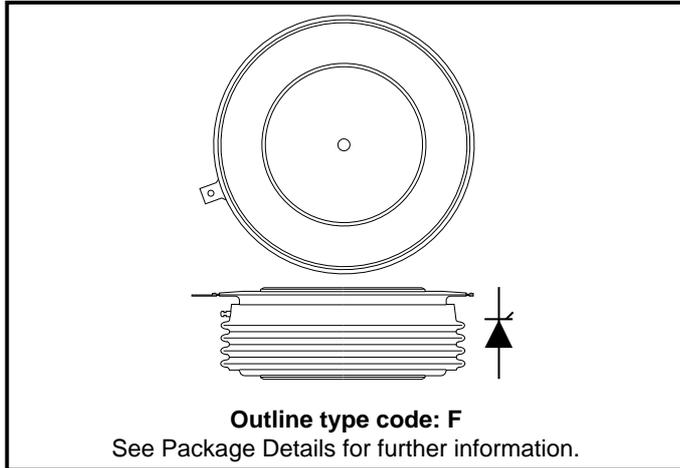


Fig. 1 Package outline

### KEY PARAMETERS

$V_{DRM}$	<b>1400V</b>
$I_{T(AV)}$	<b>1850A</b>
$I_{TSM}$	<b>32500A</b>
$dV/dt^*$	<b>1000V/<math>\mu</math>s</b>
$dI/dt$	<b>1000A/<math>\mu</math>s</b>

\*Higher dV/dt selections available

### VOLTAGE RATINGS

Part Number	Repetitive Peak Voltages	Conditions
	$V_{DRM}$ $V_{RRM}$	
	V	
DCR1002SF14	1400	$T_{vj} = 0^\circ$ to $125^\circ$ C. $I_{DRM} = I_{RRM} = 100$ mA. $V_{DRM}^* V_{RRM} = 10$ ms 1/2 sine. $V_{DSM}$ & $V_{RSM} = V_{DRM}$ & $V_{RRM} + 100$ V respectively.

Lower voltage grades available.

### ORDERING INFORMATION

When ordering, use part number shown in the Voltage Ratings table.

If a lower voltage grade is required, then use  $V_{DRM}/100$  for the grade required e.g.:

**DCR1002SF08** for an 800V device.

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

**CURRENT RATINGS**

$T_{case} = 60^{\circ}\text{C}$  unless stated otherwise.

Symbol	Parameter	Conditions	Max.	Units
<b>Double Side Cooled</b>				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	1850	A
$I_{T(RMS)}$	RMS value	-	2900	A
$I_T$	Continuous (direct) on-state current	-	2668	A
<b>Single Side Cooled (Anode side)</b>				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	1190	A
$I_{T(RMS)}$	RMS value	-	1870	A
$I_T$	Continuous (direct) on-state current	-	1550	A

**CURRENT RATINGS**

$T_{case} = 80^{\circ}\text{C}$  unless stated otherwise.

Symbol	Parameter	Conditions	Max.	Units
<b>Double Side Cooled</b>				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	1430	A
$I_{T(RMS)}$	RMS value	-	2245	A
$I_T$	Continuous (direct) on-state current	-	1780	A
<b>Single Side Cooled (Anode side)</b>				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	900	A
$I_{T(RMS)}$	RMS value	-	1414	A
$I_T$	Continuous (direct) on-state current	-	1065	A

**SURGE RATINGS**

Symbol	Parameter	Conditions	Max.	Units
$I_{TSM}$	Surge (non-repetitive) on-state current	10ms half sine; $T_{case} = 125^{\circ}C$	26	kA
$I^2t$	$I^2t$ for fusing	$V_R = 50\% V_{RRM} - 1/4$ sine	$3.38 \times 10^6$	A <sup>2</sup> s
$I_{TSM}$	Surge (non-repetitive) on-state current	10ms half sine; $T_{case} = 125^{\circ}C$	32.5	kA
$I^2t$	$I^2t$ for fusing	$V_R = 0$	$5.28 \times 10^6$	A <sup>2</sup> s

**THERMAL AND MECHANICAL DATA**

Symbol	Parameter	Conditions		Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	dc	-	0.018	$^{\circ}C/W$	
		Single side cooled	Anode dc	-	0.036	$^{\circ}C/W$	
			Cathode dc	-	0.036	$^{\circ}C/W$	
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 20kN with mounting compound		Double side	-	0.003	$^{\circ}C/W$
				Single side	-	0.006	$^{\circ}C/W$
$T_{vj}$	Virtual junction temperature	On-state (conducting)		-	135	$^{\circ}C$	
		Reverse (blocking)		-	125	$^{\circ}C$	
$T_{stg}$	Storage temperature range			-55	125	$^{\circ}C$	
-	Clamping force			18	22	kN	

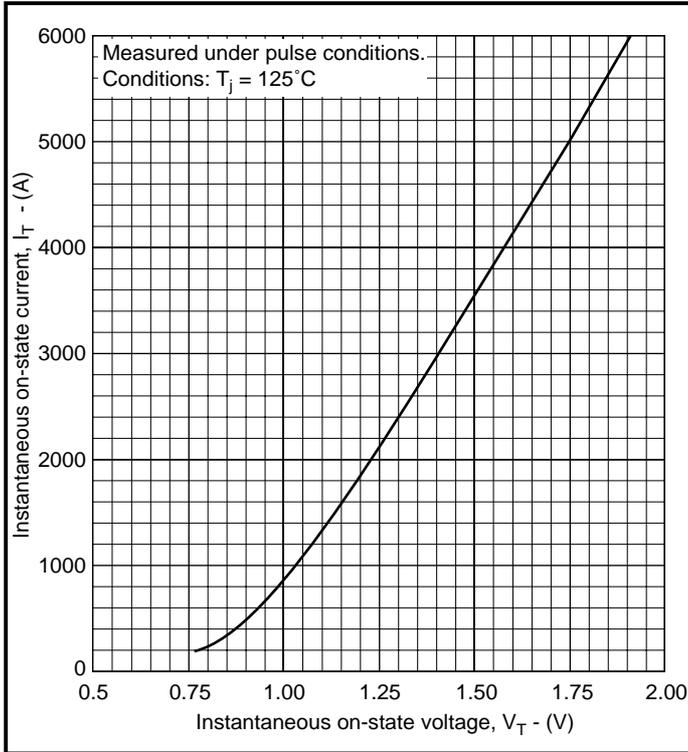
## DYNAMIC CHARACTERISTICS

Symbol	Parameter	Conditions	Max.	Units	
$I_{RRM}/I_{DRM}$	Peak reverse and off-state current	At $V_{RRM}/V_{DRM}$ , $T_{case} = 125^{\circ}C$	100	mA	
dV/dt	Maximum linear rate of rise of off-state voltage	To 67% $V_{DRM}$ , $T_j = 125^{\circ}C$ .	1000	V/ $\mu$ s	
dl/dt	Rate of rise of on-state current	From 67% $V_{DRM}$ to 1000A Gate source 20V, 10 $\Omega$ $t_r \leq 0.5\mu$ s to 1A, $T_j = 125^{\circ}C$ .	Repetitive 50Hz	500	A/ $\mu$ s
			Non-repetitive	1000	A/ $\mu$ s
$V_{T(TO)}$	Threshold voltage	At $T_{vj} = 125^{\circ}C$	0.9	V	
$r_T$	On-state slope resistance	At $T_{vj} = 125^{\circ}C$	0.17	m $\Omega$	
$t_{gd}$	Delay time	$V_D = 67\% V_{DRM}$ , Gate source 30V, 15 $\Omega$ $t_r \leq 0.5\mu$ s, $T_j = 25^{\circ}C$	2	$\mu$ s	
$t_q$	Turn-off time	$I_T = 800A$ , $t_p = 1ms$ , $T_j = 125^{\circ}C$ , $V_{RM} = 50V$ , $dl_{RR}/dt = 20A/\mu$ s, $V_{DR} = 67\% V_{DRM}$ , $dV_{DR}/dt = 20V/\mu$ s linear	200	$\mu$ s	
$I_L$	Latching current	$T_j = 25^{\circ}C$ , $V_D = 5V$	1000	mA	
$I_H$	Holding current	$T_j = 25^{\circ}C$ , $R_{g-k} = \infty$	300	mA	

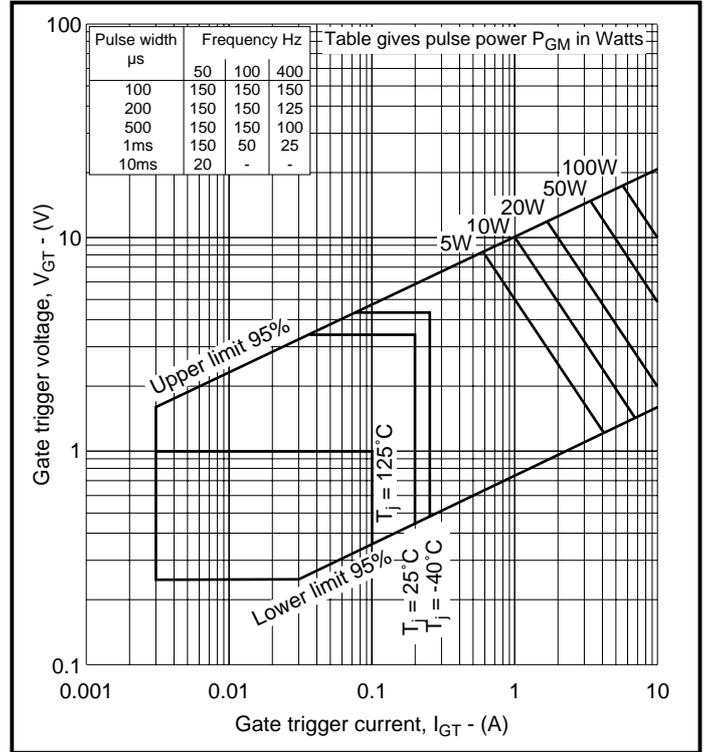
## GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Conditions	Max.	Units
$V_{GT}$	Gate trigger voltage	$V_{DRM} = 5V$ , $T_{case} = 25^{\circ}C$	3.5	V
$I_{GT}$	Gate trigger current	$V_{DRM} = 5V$ , $T_{case} = 25^{\circ}C$	200	mA
$V_{GD}$	Gate non-trigger voltage	At 67% $V_{DRM}$ , $T_{case} = 125^{\circ}C$	0.25	V
$V_{FGM}$	Peak forward gate voltage	Anode positive with respect to cathode	30	V
$V_{FGN}$	Peak forward gate voltage	Anode negative with respect to cathode	0.25	V
$V_{RGM}$	Peak reverse gate voltage		5	V
$I_{FGM}$	Peak forward gate current	Anode positive with respect to cathode	30	A
$P_{GM}$	Peak gate power	See table, gate characteristics curve	150	W
$P_{G(AV)}$	Mean gate power		10	W

**CURVES**



**Fig.2 Maximum (limit) on-state characteristics**



**Fig.3 Gate characteristics**

$V_{TM}$  Equation:-

$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where

- A = -0.6475
- B = 0.3079
- C = 0.0002787
- D = -0.02311

These values are valid for  $T_j = 125^\circ\text{C}$  for  $I_T$  500A to 6000A.

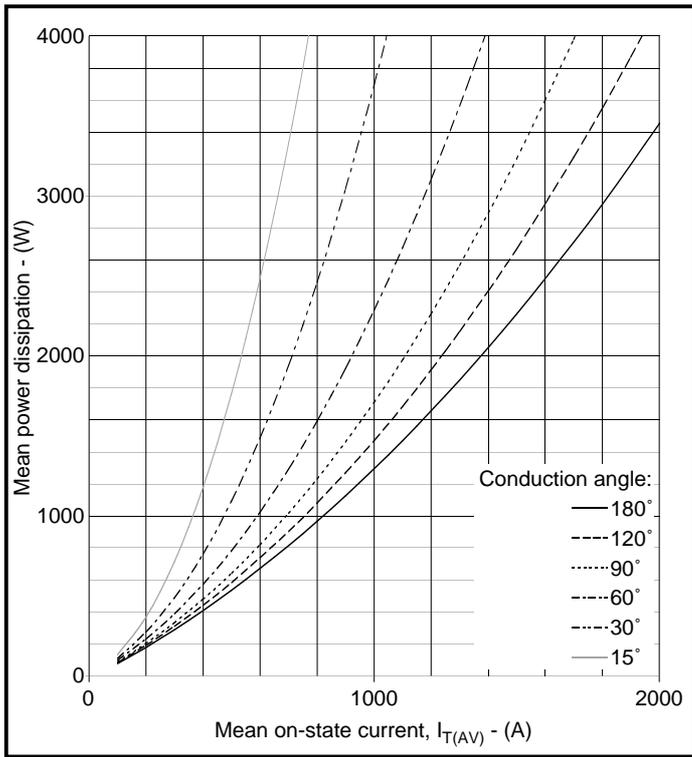


Fig.4 Power dissipation curves - sine wave

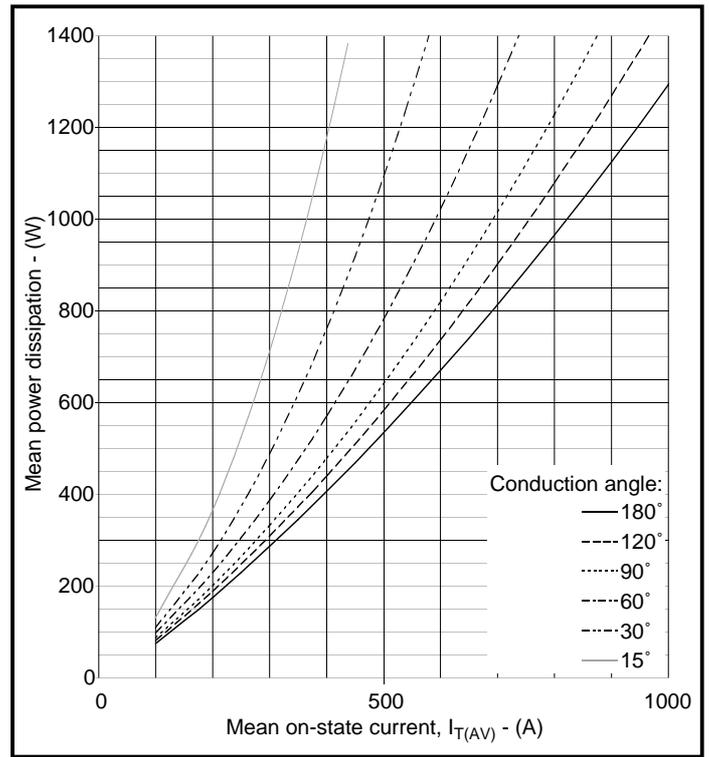


Fig.5 Power dissipation curves - sine wave

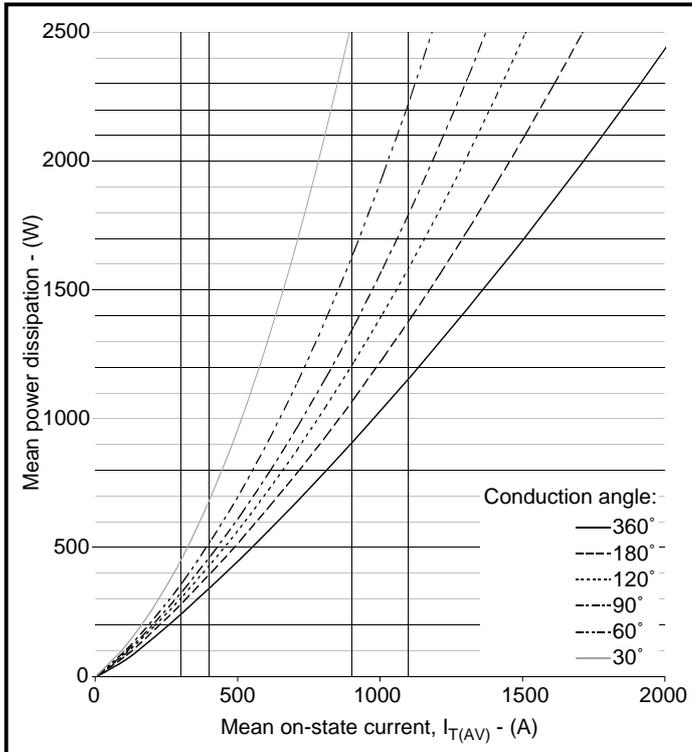


Fig.6 Power dissipation curves - square wave

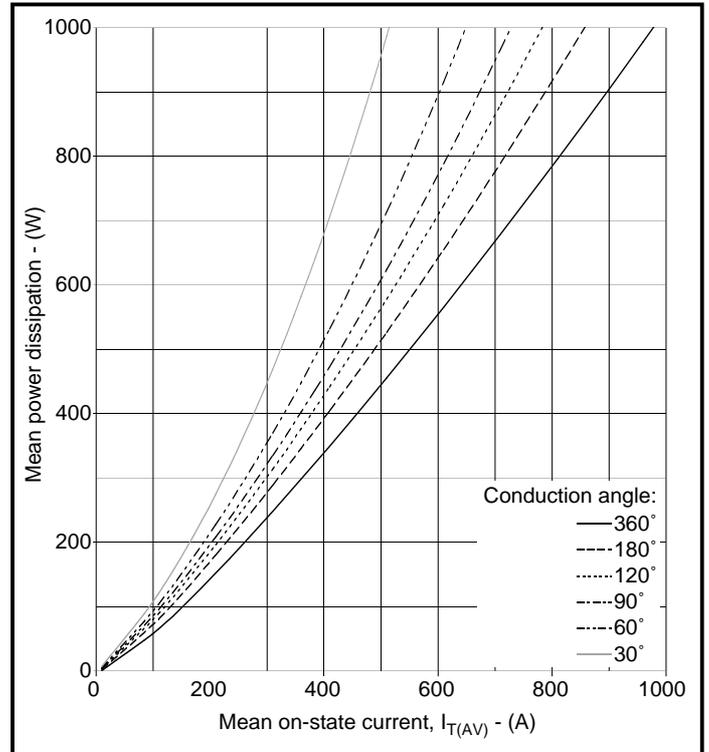
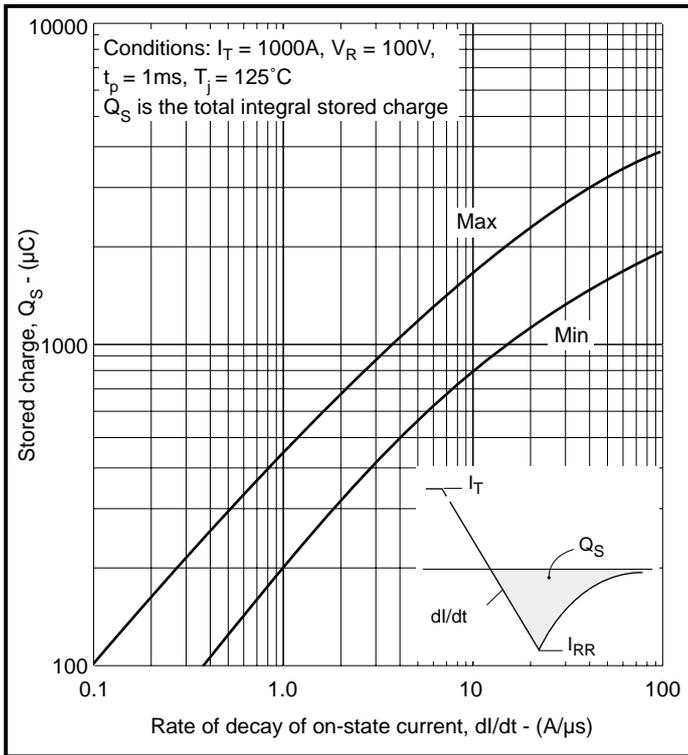
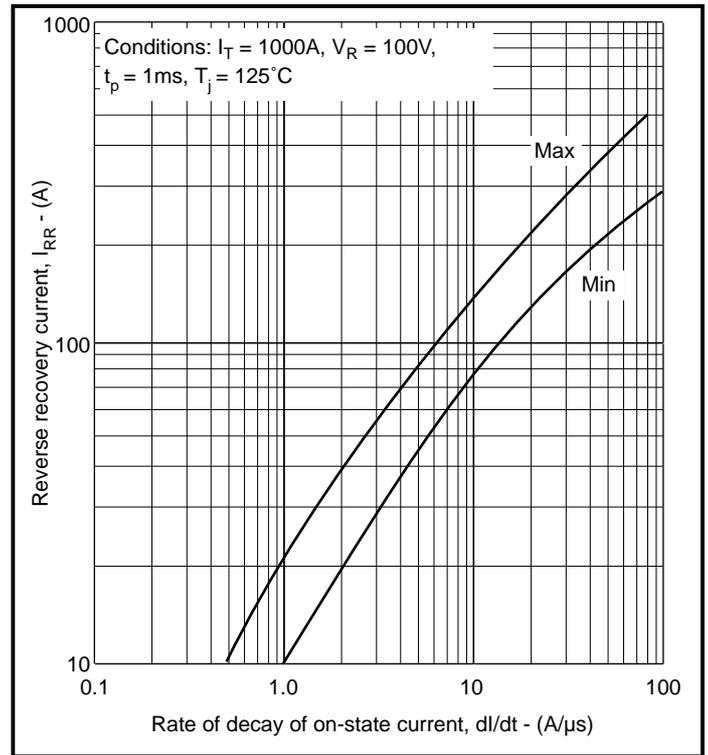


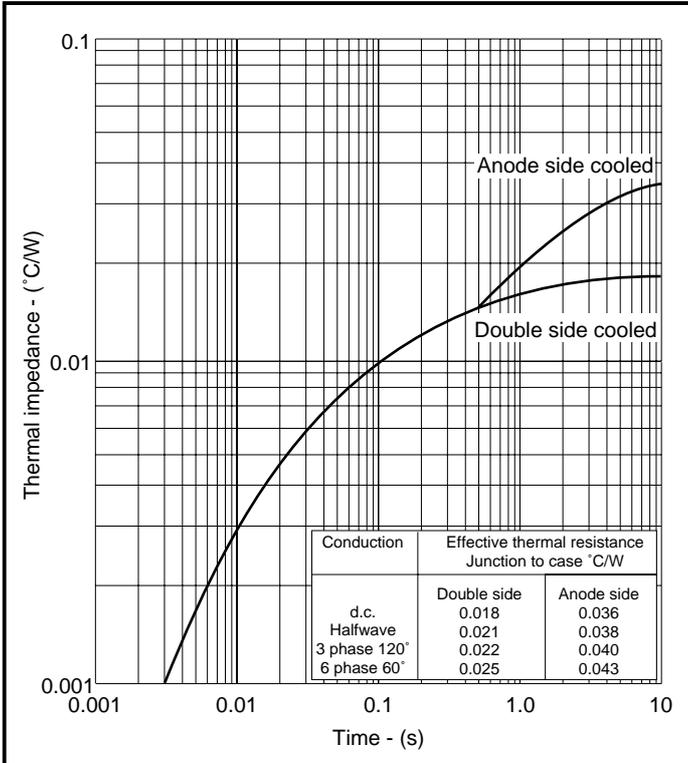
Fig.7 Power dissipation curves - square wave



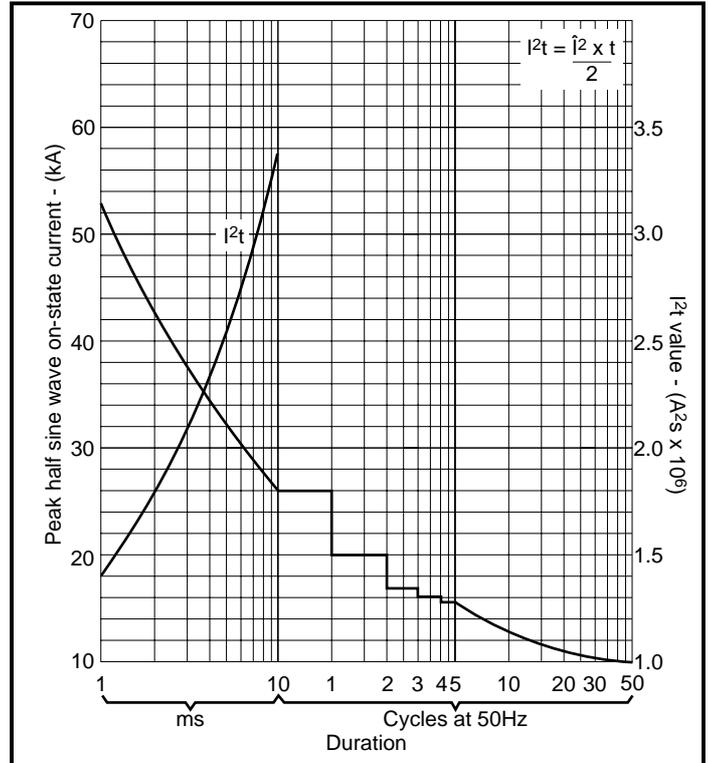
**Fig.8 Stored charge**



**Fig.9 Reverse recovery current**



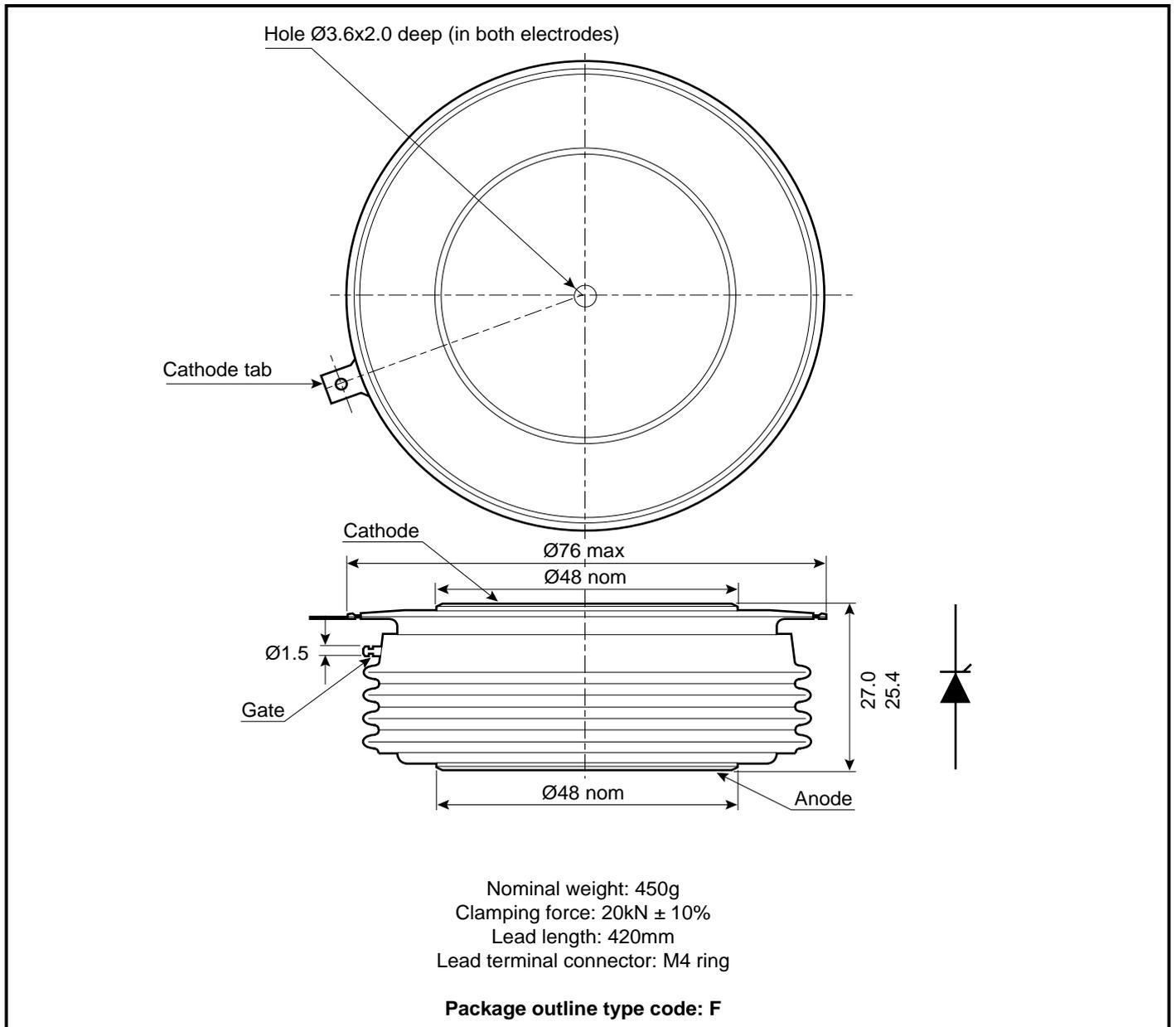
**Fig.10 Transient thermal impedance - junction to case**



**Fig.11 Surge (non-repetitive) on-state current vs time (with 50%  $V_{RRM}$  at  $T_{case} = 125^\circ C$ )**

**PACKAGE DETAILS**

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



**Fig.12 Package details**

## POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

## HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.



<http://www.dynexsemi.com>

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**Preliminary Information:** The product is in design and development. The datasheet represents the product as it is understood but details may change.

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